Lecture 12 - Microwave Transistors

Microwave Active Circuit Analysis and Design

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Academic Press Inc.



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Intended Learning Outcomes

Knowledge

- Be familiar with the specific types of transistors used at microwave frequencies and their various limitations.
- Understand the origins of equivalent circuit models for microwave bipolar and field effect transistors.
- Understand the multi-layered construction of MMICs how passive components can be constructed in MMIC form.
- Skills
 - Be able to distinguish between a BJT, HBT, MESFET and HEMT transistor types, and be able to explain the basic operation of these devices and their relative performance characteristics.
 - Be able to draw the equivalent circuit of a BJT/HBT and a MESFET/HEMT and be able to explain physical origin of equivalent circuit components, including parasitics.
 - Be able to estimate the f_T and f_{max} of a given transistor type, with given equivalent circuit component values.
 - Be able to identify the main passive component types used in contemporary MMIC design and their equivalent circuits.

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BJT construction

- The basic construction of a planar epitaxial BJT is shown in figure 1. The device consists of three differently doped semiconductor regions, the emitter region, the base region and the collector region.
- The term *epitaxial* refers to the fact that the device is constructed by the deposition of successive crystalline layers on top of a crystalline substrate.
- The three regions in figure 1 are, respectively, n-type, p-type and n-type in a npn transistor and p-type, n-type and p-type in a pnp transistor. Metal contacts connects the respective semiconductor region to the external circuit.

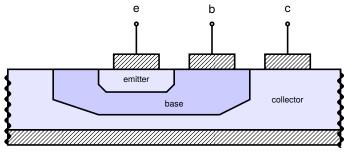
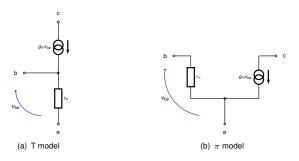
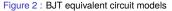


Figure 1 : Conceptual BJT cross-section

The BJT equivalent circuit

For small signal currents and voltages, the BJT may be represented by two alternative equivalent circuits called the the *T*-model and the π -model respectively, as shown in figure 2.





- r_π is the small signal active mode input resistance seen looking into the base, with emitter grounded.
- r_e is the small signal active mode input resistance seen looking into the emitter, with the base grounded.

 r_e and r_{π} are related by[4]:

$$r_{\pi} = (1 + \beta)r_{\theta} \tag{1}$$

The BJT equivalent circuit

The inverse of g_m has the dimensions of resistance, i.e. $1/g_m = r_e$. The resistance r_e , as shown in 2(a), is known as the *dynamic resistance* of the base-emitter junction, and its value is a function of both current (hence the adjective 'dynamic'), and the temperature of the device.

A good approximation of r_e is given by:

$$r_e \approx \frac{25}{l_e(mA)}\Omega$$
 (2)

For more detained explanation and derivation of these terms the reader may consult some of the general texts on this subject[18, 7, 4].

By application of (2) we get some typical values of r_e as follows :

Table 1 : Approximate values of g_m and r_e versus I_e

l _e	g _m	r _e
1 <i>mA</i>	40 <i>mS</i>	25Ω
10 <i>mA</i>	400 <i>mS</i>	2.5Ω
25 <i>mA</i>	1,000 <i>mS</i>	1Ω

High frequency BJT performance

At higher frequencies, the gain of the transistor drops off with frequency due to charge storage effects within the various regions of the device. These effects can be modelled by adding parasitic capacitors to the low frequency π model of figure 2(b). The resulting equivalent circuit, commonly referred to as the *hybrid* π model is shown in figure 3, which represents the intrinsic device alone, without package parasitics.

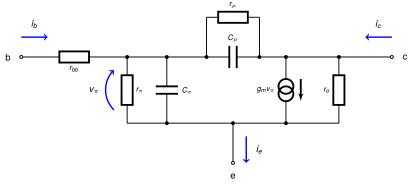


Figure 3 : BJT hybrid π model equivalent circuit

High frequency BJT performance

The elements that have been added in figure 3 are as follows:

- 1. Base-emitter capacitance (C_{π}) : includes the base-emitter diffusion capacitance and the base-emitter junction capacitance. In microwave transistors, this combined capacitance ranges from a few femto-Farads (fF) to a few pico-Farads (pF).
- 2. Collector-base feedback capacitance (C_{μ}) : representing the junction capacitance across the reverse biased collector-base junction. Because the junction is reverse biased, under normal operating conditions there is no diffusion capacitance in this case. Although this capacitor is usually small, less than 1pF, its influence is multiplied by the transistor gain which amplifies the voltage variation at the base connection and applies it to the collector connection, exaggerating the influence of this capacitor through the Miller effect, which was discussed in chapter **?**
- 3. Intrinsic base-collector resistance (r_{μ}) : representing the resistance between the collector and the base when the junction is under reverse bias. It is thus usually a high value (hundreds of $k\Omega$ to several $M\Omega$).
- 4. Base spreading resistance (*r_{bb}*): representing the resistance between the base metal contact and the active region of the semiconductor material making up the base region of BJT. For a microwave transistor its value ranges from a few ohms to tens of ohms.
- 5. Intrinsic base-emitter resistance r_{π} : the internal resistance of the forward biased base-emitter junction, as described in section **??**. Its value is a function of the current gain of the device and the operating current.
- 6. Output resistance (*r_o*): representing the bulk resistance of the material between collector and the emitter. It is usually quite high, in the order of 100kΩ. *r_o* is also a dynamic resistance as it is a function of the variation of the collector current with the transistor bias voltages. This phenomenon is referred to as the *Early effect*[18].

BJT cut off frequency

The cut off frequency, f_T , for a BJT can be calculated from the circuit shown in figure 3. If we apply a short-circuit between the collector to the emitter, so as to measure i_c , we find that the base-emitter voltage, v_{π} , is also applied across C_{μ} . Hence we can write :

$$i_b = \frac{v_\pi (1 + j\omega r_\pi C_\pi)}{r_\pi} \tag{3}$$

$$i_c = (g_m - j\omega C_\mu) v_\pi \tag{4}$$

For the frequency range for which this model is valid, ωC_{μ} is much less than g_m and, therefore, we can calculate the short-circuit current gain as follows:

$$\frac{i_c}{i_b} \approx \frac{g_m r_\pi}{1 + j\omega (C_\mu + C_\pi) r_\pi}$$
(5)

If $\omega_T = 2\pi f_T$ is the frequency for which the current gain is unity, i.e.

$$\left|\frac{i_c}{i_b}\right| = 1 \tag{6}$$

BJT cut off frequency

then, at $\omega = \omega_T$ we can write :

$$\frac{g_m r_\pi}{\sqrt{1 + \omega_T^2 (C_\mu + C_\pi)^2 r_\pi^2}} = 1$$
(7)

Hence:

$$1 + \omega_T^2 (C_\mu + C_\pi)^2 r_\pi^2 = (g_m r_\pi)^2$$
(8)

Which yields ω_T as follows:

$$\omega_T^2 = \frac{(g_m r_\pi)^2 - 1}{(C_\mu + C_\pi)^2 r_\pi^2} \tag{9}$$

Since $(g_m r_\pi)^2 >> 1$ we can write:

$$\omega_T \approx \frac{g_m}{C_\mu + C_\pi} \tag{10}$$

Thus, the unity-gain bandwidth, f_T , of a BJT can be approximated, in terms of the hybrid- π model parameters as follows:

$$\left| f_{T} \approx \frac{g_{m}}{2\pi (C_{\mu} + C_{\pi})} \right|$$
(11)

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f_{max} versus f_T for a BJT

 f_T is also known as the *gain bandwidth product*, a term which emphasises the trade-off between current gain, which is proportional to g_m , and bandwidth, which is proportional to $1/(C_{\pi} + C_{\mu})$. For microwave transistors, f_T , in the range of tens to hundreds of GHz depending on the device technology. Since g_m is proportional to collector current, i_c , the gain bandwidth product has to be specified at a particular value of collector current.

Though common emitter current gain is equal to unity at f_T , by definition, there may still be considerable power gain at f_T due to different input and output matching conditions. Thus, f_T does not necessarily represent the highest useful frequency of operation of a transistor. Another figure of merit, the *maximum frequency of oscillation*, (f_{max}), is often used. f_{max} is the frequency at which common emitter power gain is equal to unity and is related to f_T as follows[15]:

$$f_{max} = \sqrt{\frac{f_T}{8\pi r_{bb}C_{\mu}}} \tag{12}$$

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Although f_{max} will generally be higher than f_T , we should not always assume that this is the case. Since f_T is a measure of voltage gain whereas f_{max} is a measure of power gain, a transistors that still has a voltage gain greater than unity above f_{max} will have $f_T > f_{max}[17]$.

BJT high frequency hybrid- π equivalent circuit

Figure 4 shows the addition of package parasitics to the intrinsic BJT equivalent circuit of figure 3.

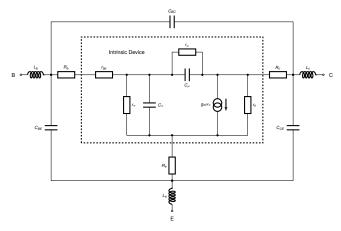


Figure 4 : BJT hybrid π model equivalent circuit with package parasitics

BJT high frequency hybrid- π equivalent circuit

By way of illustration, hybrid- π parameters for a typical microwave BJT are shown in table 2 and table 3[14]:

Model parameters for a typical microwave BJT

Table 3 : Extrinsic parameters

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			Le	> 100 <i>pH</i>
g _m	$80mS(@I_C = 2mA)$		Lc	> 100 <i>pH</i>
r _{bb}	38Ω		Lb	> 100 <i>pH</i>
rπ	1.1 <i>k</i> Ω		C_{BC}	> 20 <i>fF</i>
r_{μ}	270kΩ		C_{BE}	> 20 <i>fF</i>
\dot{C}_{π}	130 <i>fF</i>		C_{CE}	> 20 <i>fF</i>
\mathcal{C}_{μ}	8fF		re	3.4Ω
ro	$5M\Omega$		r _c	2.0Ω
		1	r _b	3.8Ω

Table 2 : Intrinsic parameters

Applying (11) to the intrinsic device in table 2, we get an f_T of around 92GHz. Applying (12) gives the f_{max} of the intrinsic device as around 110GHz.

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Recapping the definition of the *h*-parameters from section **??** we have, for the common emitter configuration :

 $\begin{array}{c}
 h_{ie} = \frac{v_{be}}{i_b} \Big|_{v_{ce}=0} \\
 h_{re} = \frac{v_{be}}{v_{ce}} \Big|_{i_b=0} \\
 h_{fe} = \frac{i_c}{i_b} \Big|_{v_{ce}=0} \\
 h_{oe} = \frac{i_c}{v_{ce}} \Big|_{i_b=0}
\end{array}$ (13)

In other words, we measure the parameters h_{ie} and h_{fe} with the output short circuited, whereas the parameters h_{re} and h_{oe} are measured with the input open circuited.

Applying a short circuit at the output of figure 3 we can therefore write :

$$h_{ie} = \frac{v_{be}}{i_b} = r_{bb} + \frac{r_{\pi}}{1 + j\omega r_{\pi}(C_{\mu} + C_{\pi})}$$
(14)

where r_x is the parallel combination of r_{π} and r_{μ} , i.e. :

$$r_{\rm X} = \frac{r_{\pi}r_{\mu}}{r_{\pi} + r_{\mu}} \tag{15}$$

Since, in general, $r_{\pi} \ll r_{\mu}$, we can write:

$$h_{ie} \approx r_{bb} + \frac{r_{\pi}}{1 + j\omega r_{\pi}(C_{\mu} + C_{\pi})}$$
(16)

It is also usually the case that $C_{\pi} >> C_{\mu}$, so (16) can be further simplified to:

$$h_{ie} = r_{bb} + \frac{r_{\pi}}{1 + j\omega r_{\pi} C_{\pi}}$$
(17)

With the output short circuited and applying the same approximations with regard to r_{μ} and C_{μ} as above, we can determine h_{fe} by establishing the relationship between v_{be} and i_b in figure 3 as follows:

$$v_{be} = \frac{i_b r_\pi}{1 + j\omega r_\pi (C_\mu + C_\pi)} \approx \frac{i_b r_\pi}{1 + j\omega r_\pi C_\pi}$$
(18)

Noting that $i_c = g_m i_b$ we can write:

$$h_{fe} = \frac{i_c}{i_b} = \frac{g_m v_{be}}{i_b} \tag{19}$$

Combining (18) and (19) gives :

$$h_{fe} = \frac{g_m r_\pi}{1 + j\omega r_\pi C_\pi}$$
(20)

To compute the parameters h_{re} and h_{oe} we now apply an open circuit to the input. Applying a hypothetical voltage generator to this input we can write:

$$h_{re} = \frac{v_{be}}{v_{ce}} = \frac{\left(\frac{r_{\pi}}{1+j\omega r_{\pi}C_{\pi}}\right)}{\left(\frac{r_{\pi}}{1+j\omega r_{\pi}C_{\pi}}\right) + \left(\frac{r_{\mu}}{1+j\omega r_{\mu}C_{\mu}}\right)}$$
(21)

Applying the same approximations with regard to r_{μ} and C_{μ} as above, we can approximate (21) as follows:

$$h_{re} \approx \left(\frac{r_{\pi}}{r_{\mu}}\right) \cdot \frac{1 + j\omega r_{\mu} \mathcal{C}_{\mu}}{1 + j\omega r_{\pi} \mathcal{C}_{\pi}}$$
(22)

Finally, we determine the parameter h_{oe} by reference to figure 3 as follows :

$$h_{oe} = \frac{i_c}{v_{ce}} = \frac{1}{r_o} + \frac{1}{\left(\frac{r_{\mu}}{1+j\omega r_{\mu}C_{\mu}}\right) + \left(\frac{r_{\pi}}{1+j\omega r_{\pi}C_{\pi}}\right)} + g_m\left(\frac{r_{\pi}}{r_{\mu}}\right) \cdot \frac{1+j\omega r_{\mu}C_{\mu}}{1+j\omega r_{\pi}C_{\pi}}$$
(23)

The last term is a result of the presence of the current generator. This term can be written as $g_m h_{re}$.

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Applying this, and the approximations with regard to r_{μ} and C_{μ} , we can rewrite (23) as follows:

$$h_{oe} \approx \frac{1}{r_o} + \frac{1}{r_{\mu}} + j\omega C_{\mu} + g_m \left(\frac{r_{\pi}}{r_{\mu}}\right) + \frac{g_m \left(1 - \frac{r_{\pi}C_{\pi}}{r_{\mu}C_{\mu}}\right) \frac{C_{\mu}}{C_{\pi}} j\omega}{j\omega + \frac{1}{r_{\pi}C_{\pi}}}$$
(24)

Since $r_{\pi}r_{\mu} >> r_{\pi}C_{\pi}$ we can make the approximation:

$$\left(1 - \frac{r_{\pi} C_{\pi}}{r_{\mu} C_{\mu}}\right) \approx 1 \tag{25}$$

(24) can now be approximated as:

$$h_{oe} \approx \frac{1}{r_o} + \frac{1}{r_\mu} + j\omega C_\mu + g_m \left[\frac{r_\pi}{r_\mu} + \frac{j\omega C_\mu}{\frac{1}{r_\pi} + j\omega C_\pi} \right]$$
(26)

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Heterojunction Bipolar Transistor (HBT)

The Heterojunction Bipolar Transistor (HBT) is a type of bipolar junction transistor (BJT) that uses a different type of semiconductor material for the emitter and base regions, creating a *heterojunction*.

There are two versions of HBT, the Single Heterojunction Bipolar Transistor (SHBT) and the Double Heterojunction Bipolar Transistor (DHBT) as shown in figure 5.

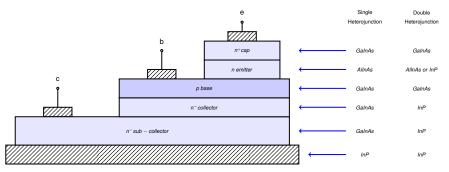


Figure 5 : Simplified conceptual Heterojunction Bipolar Transistor (HBT) cross-section with materials

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Metal-Semiconductor Field Effect transistor (MESFET)

A simplified illustration of the structure of a MESFET is shown in figure 6.

- The device consists of a channel of semiconducting material positioned between source and drain regions. The carrier flow from source to drain is controlled by the voltage applied to the gate electrode.
- ► The controlled current flows only through the thin *n*-type channel between the two highly doped *n*⁺ regions, meaning that MESFETs are *unipolar* devices.
- The main advantage of a unipolar device is that the the charge storage phenomenon seen in the base region of a conventional BJT is eliminated.
- It is this charge storage which primarily limits the high frequency performance of bipolar devices. The control of the channel is effected by varying the depletion layer width underneath the metal contact which modulates the thickness of the conducting channel and thereby the current between source and drain.

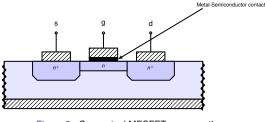


Figure 6 : Conceptual MESFET cross-section

High Electron Mobility Transistors (HEMT)

The High Electron Mobility Transistors (HEMT) is basically the heterojunction approach applied to the MESFET topology. This means that the channel region of the FET is constructed of two materials with different band gaps instead of a doped region of single material in the case for the simple MESFET, an approach known as *modulation doping*[5]. The heterojunction approach results in higher electron mobility in the channel, allowing the device to respond to rapid changes in the gate voltage.

A simplified illustration of the structure of a HEMT is shown in figure 7.

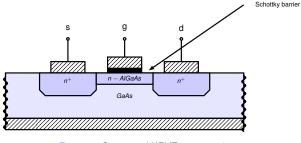


Figure 7 : Conceptual HEMT cross-section

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MESFET and HEMT equivalent circuit

The first equivalent circuit derived specifically for the GaAs MESFET by considering both the intrinsic and extrinsic elements was proposed by Wolf[20] and is shown in figure 8.

The physical meaning of the various components in figure 8 are as follows:

- 1. C_{gs} and C_{gd} correspond to the gate-source and gate-drain junction capacitances respectively.
- 2. C_l and C'_d correspond to the extrinsic gate-source and drain-source capacitances.
- 3. *R_i* is the resistance of the ohmic channel between the source and the gate.
- g_m represents the steady-state transconductance of the device, which is frequency dependent (see below).
- 5. R_{ds} is the channel resistance between the drain and the source.

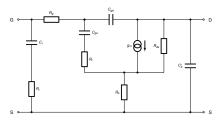


Figure 8 : MESFET equivalent circuit due to Wolf[20]

MESFET and HEMT equivalent circuit

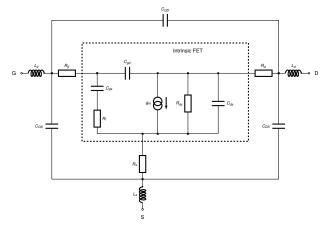


Figure 9 : MESFET or HEMT equivalent circuit with package parasitics

Typical MESFET equivalent circuit parameters

By way of illustration, the equivalent circuit parameters for a typical microwave MESFET, calculated from S-parameter measurements and with reference to figure 9 are shown in table 4 and table 5[1, 8, 13]:

Model parameters for a typical microwave MESFET

Table 4 : Intrinsic parameters

g _m	45 <i>mS</i>
τ	6pS
Ri	0.5Ω
R _{ds}	1.1 <i>k</i> Ω
C_{gs}	0.55 <i>pF</i>
C _{gd}	0.04 <i>pF</i>
C _{ds}	0.15 <i>pF</i>

Table 5 : Extrinsic parameters

10 <i>pH</i>
'
460pH
340pH
70 <i>fF</i>
70 <i>fF</i>
70 <i>fF</i>
3.4Ω
2.0Ω
3.8Ω

We can obtain the Y-parameters of the intrinsic FET in figure 9, after de-embedding the device from the extrinsic parasitics[6, 3, 12] by straightforward circuit analysis. Recall the definition of Y-parameters from section?? as follows:

$$Y_{11} = \frac{i_1}{v_1} \Big|_{v_2 = 0}$$

$$Y_{12} = \frac{i_1}{v_2} \Big|_{v_1 = 0}$$

$$Y_{21} = \frac{i_2}{v_1} \Big|_{v_2 = 0}$$

$$Y_{22} = \frac{i_2}{v_2} \Big|_{v_1 = 0}$$

(27)

By inspection of the intrinsic equivalent circuit in figure 9 and applying the definitions of 27, we can write:

$$Y_{11} = \frac{\omega^2 C_{gs}^2 R_i^2}{1 + \omega^2 C_{gs}^2 R_i^2} + j\omega \left(\frac{C_{ds}}{1 + \omega^2 C_{gs}^2 R_i^2} + C_{dg}\right)$$
(28)

$$Y_{12} = -j\omega C_{dg} \tag{29}$$

$$Y_{21} = \frac{g_{m_0} e^{-j\omega\tau}}{1 + j\omega C_{gs} R_i} - j\omega C_{gd}$$
(30)

$$Y_{22} = \frac{1}{R_{ds}} + j\omega(C_{ds} + C_{gd})$$
(31)

Taking the Y-parameter expressions (28) to (31), and separating them into real and imaginary parts, the various intrinsic equivalent circuit elements can be found analytically as shown on the next slide[1, 9]:

$$C_{dg} = \frac{-lm(Y_{21})}{\omega} \tag{32}$$

$$C_{ds} = \frac{Im(Y_{22}) - \omega C_{dg}}{\omega}$$
(33)

$$C_{ds} = \frac{Im(Y_{11}) + Im(Y_{12})}{\omega} \left[1 + \frac{Re(Y_{12})^2}{(Im(Y_{11}) + Im(Y_{12}))^2} \right]$$
(34)

$$R_{i} = \frac{Re(Y_{11})}{Re(Y_{11})^{2} + (Im(Y_{11}) + Im(Y_{12}))^{2}}$$
(35)

$$g_m = \sqrt{(1 + \omega^2 R_i^2 C_{gs}^2) Re(Y_{21})^2 + (Im(Y_{22}) + \omega C_{dg})^2}$$
(36)

$$G_{ds} = Re(Y_{22}) \tag{37}$$

$$\tau = \frac{1}{\omega} \arctan\left[\frac{-Im(Y_{21}) - \omega R_i C_{gs} Re(Y_{21}) - \omega C_{gd}}{Re(Y_{21}) - \omega R_i C_{gs} Im(Y_{21}) - \omega^2 R_i C_{gs} C_{dg}}\right]$$
(38)

Analysis of the intrinsic equivalent circuit shown in figure 9 yields the following expression for the gain-bandwidth product of the MESFET, which is similar in form to that for a BJT given in (??):

$$f_T \approx \frac{g_m}{2\pi (C_{gs} + C_{gd})} \tag{39}$$

As with the case of BJTs, f_T does not necessarily represent the highest useful frequency of operation of a MESFET as there may be useful power gain that can be extracted even above f_T . We therefore need a definition of f_{max} , the maximum oscillation frequency of a MESFET, which is as follows[19]:

$$f_{max} = \frac{f_T}{2} \sqrt{\frac{R_{ds}}{R_i + R_g + R_s}}$$
(40)

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Monolithic Microwave Integrated Circuits (MMICs)

A GaAs MMIC is composed of several layers, all structures are built on a semi-insulating GaAs substrate. The semi-insulating nature of GaAs allows the easy integration of various passive components. A typical process can include eight or more layers of ion implanted GaAs, dielectric insulator layer(s) and metallisation layer(s)

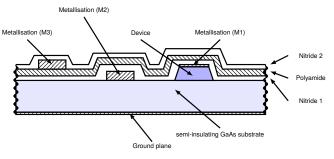


Figure 10 : Typical MMIC cross-sectional view

Monolithic Microwave Integrated Circuits (MMICs)

- 1. The active layer: usually two levels of doping (sub-layers) define the active device; n active sub-layer (doping density $\approx 10^{17}/cm^3$) and n^+ low resistance contact sub-layer (doping density $\approx 10^{18}/cm^3$).
- 2. Ohmic contact layer (M1 in figure 10): made of a high conductivity metal alloy, such as AuGe-Ni-Au, is commonly used for contacts to the *n*+ layers of MESFETs drain and source terminals.
- Schottky (gate) metallisation: This is the layer that defines the gates of the MESFETs. The gate metallisation is applied after the gate region is recessed to provide the appropriate pinch-off voltage. Metallisation is applied in three (or more) metal layers (Ti, Pt, Au).
- 4. Second metal layer (M2 in figure 10): Alloy metals are used to form contacts to the ohmic contact layer and to form the lowest layer of Metal-Insulator-Metal (MIM) capacitors.
- 5. Dielectric layers: usually Silicon Nitride (SiN) or polymide, are used for passivation of exposed semiconductor layers and as a dielectric layer for MIM capacitors.
- Third metal layer (M3 in figure 10): few microns thick (low resistance) metal used to form top layers of MIM capacitors, interdigital capacitors, spiral inductors, transmission lines and other interconnect components such as air bridges.
- 7. Ground plane: In many MMICs the underside of the thinned wafer is metallised to form a ground plane.

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MMIC MESFETs

The MESFET is built on the two active sub-layers of the GaAs substrate. The operational characteristics of a given MESFET are strongly dependent on its geometry and size. A cross section of a typical MESFET is shown in figure 11.

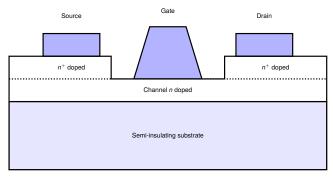


Figure 11 : Typical MESFET structure

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MMIC MESFETs

One of the most common gate cascading geometries is known as the ' Π -geometry', where several gate lines, also known as gate 'fingers', are connected together. This is shown in figure 12.

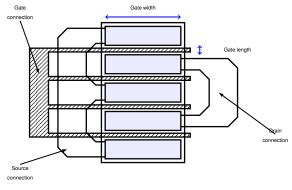


Figure 12 : Typical MESFET layout (4 finger Π-structure)

The device shown in figure 12 can be viewed as a cascade of four identical MESFETs each having a single gate finger. The Π -geometry is used to reduce the overall lateral size of the MESFET.

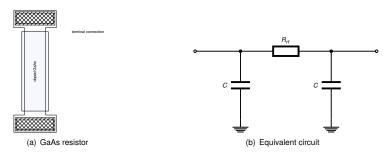
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MMIC Resistors

Two types of resistors are available in MMICs :

- The implant resistor, which is constructed by defining an area on the ion implanted semiconductor having a specific resistivity, defined by the level of doping, and using ohmic contacts for terminal connections..
- ► The *Thin Film Resistor* (TFR), which consists of a thin metallic layer of an alloy such as Nichrome (NiCr).

For both types of resistor, the value of the resistor is determined by the aspect ratio. Resistor values ranging from few Ω to 10 $k\Omega$ can be constructed by these methods. A typical structure of such a resistor, together with its equivalent circuit model are shown in figure 13 below.





The most commonly used type of MMIC capacitors is the Metal-Insulator-Metal (MIM) capacitor, also referred to as 'overlay' capacitor.

It is simply constructed by using two metallic layers with a dielectric layer, such as silicon nitride, 'sandwiched' in between. Capacitance values ranging from hundreds of femtoFarads (fF) to 100 pF can be achieved by this type of capacitor construction.

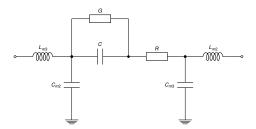


Figure 14 : MIM capacitor equivalent circuit

The primary capacitance, C, in figure 14 is given by:

$$C \approx \frac{\varepsilon_o \varepsilon_r A}{t} \tag{41}$$

Where $\varepsilon_o \varepsilon_r$ is the permittivity of the insulator, *t* is its thickness and *A* is the capacitor area.

A typical equivalent circuit model for such capacitors is shown in figure 14. The parallel conductance, *G*, is associated with leakage currents and dielectric losses. This element is often ignored in practice. The series resistance, *R*, can be calculated from the resistivity of the metal used to fabricate the capacitor, together with its geometry. L_{m3} and L_{m2} model the inductance of the capacitor terminals, while C_{m3} and C_{m2} model the fringe capacitance (to ground) of each of the overlay metal plates. These parasitic elements can be estimated by modelling the MIM capacitor as a short length of microstrip line[16].

An alternative MMIC capacitor geometry is known as the 'interdigital' or 'interdigitated' capacitor, which is a planar structure formed in one of the metallisation layers, as shown in figure 15.

This geometry is used when particularly accurate values of capacitance are required. The capacitance can be controlled by controlling the finger geometry (length, width and spacing)[10].

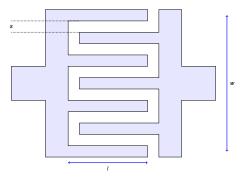


Figure 15 : Interdigital capacitor layout

The following approximate expression for the primary capacitance, *C*, of an interdigital capacitor having N > 4 fingers is given in Robertson and Lucyszyn's book[16] :

$$C = \frac{l(\varepsilon_r + 1)}{w} [(N - 3)A_1 + A_2]$$
(42)

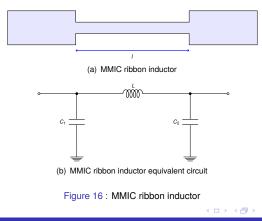
Where A_1 and A_2 are given by $8.85 \times 10^{-12} \times w$ and $9.92 \times 10^{-12} \times w$ respectively, with *w* being the total width of the structure in cm (as shown in figure 15). Equation (42) is an approximation that is valid for cases where the substrate thickness, *h*, is large in relation to the strip spacing, *s*, i.e. (h/s > 100).

MMIC Inductors

MMIC inductors are generally constructed in one of three types, depending on the value required. These are, in order of increasing inductance value:

- 1. A length of 'thin' microstrip line (a 'ribbon' inductor).
- 2. A microstrip loop.
- 3. A spiral inductor.

The ribbon inductor construction is illustrated in figure 16(a). This structure is essentially a short length of high impedance transmission line, it is therefore only valid as an inductor for short lengths, i.e. $I < \lambda_g/4$.



MMIC Inductors

Provided that $l < \lambda_g/4$ the equivalent inductance is given by:

$$L = \frac{Z_o}{2\pi f} \sin\left(\frac{2\pi l}{\lambda_g}\right) \tag{43}$$

There will inevitably be parasitic elements that will have to be taken into account in the design of such inductors. The dominant parasitics in this case will be the shunt capacitances shown in figure 16(b), whose values are given by:

$$C = \frac{1}{2\pi I Z_o} \tan\left(\frac{\pi I}{\lambda_g}\right) \tag{44}$$

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MMIC Inductors

If slightly larger inductances are required, then a microstrip loop inductor can be used, as shown in figure 17. This is essentially just a longer version of the ribbon inductor, so the equivalent circuit is the same as that shown in figure 16(b), and the values can also be calculated from (43) and (44).

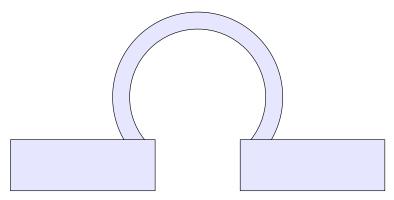


Figure 17 : Basic MMIC loop inductor

MMIC spiral inductor

The main drawback of spiral inductors is that they exhibit high frequency resonance behaviour, due to the relatively high parasitic capacitances associated with the underpass or overpass needed to obtain access to the inductor terminals.

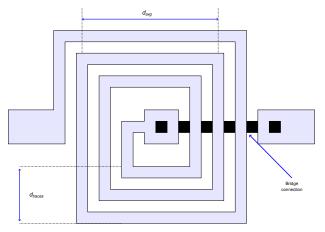
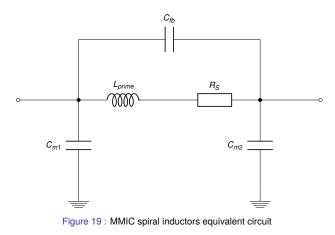


Figure 18 : MMIC spiral inductor

MMIC spiral inductor equivalent circuit

Figure 19 shows a typical equivalent circuit of a spiral inductor. The inductance of the coil is represented by L_{prime} the series resistance of the line is represented by R_S . The parallel capacitance C_{fb} represents the parasitic coupling between the parallel lines. The shunt elements C_{m1} and C_{m2} represent the capacitance between the coil and the ground planes.



MMIC spiral inductor parameters

There is a trade-off between inductance and Q for such spiral inductors. Higher inductance can be achieved by more turns, but this increases the total line length. As a consequence, the series resistance R_S as well as the parasitic coupling capacitance between the lines both increase. In addition, the inductor is limited to operate at frequencies where the total length is less than a quarter of the signal wavelength, otherwise the line will act as a resonator.

The following expression has demonstrated good accuracy for predicting the inductance of a rectangular spiral such as that shown in figure 18[11, 2]:

$$L = \frac{2\mu_o n^2 d_{avg}}{\pi} \left[\ln\left(\frac{2.067}{\rho}\right) + 0.178 + 0.125\rho^2 \right]$$
(45)

where *n* is the number of turns in the spiral, μ_o is the permeability of free space, d_{avg} represents the average diameter of the spiral, as shown in figure 18, and ρ represents the percentage of the inductor area that is filled by metal traces and is defined according to figure 18 as[2]:

$$\rho = \frac{d_{traces}}{d_{avg}} \tag{46}$$

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Equation (45) is based on a current sheet approximation of the spiral structure, and is valid only for square spirals. Interested readers are referred to the oft-cited paper by Mohan[11] also presents a range of expressions that are valid for other planar inductor geometries, such a circular spirals.

MMIC Transmission lines

- Transmission lines on MMICs are implemented as microstrip lines using one of the higher (non-ohmic) layer metals (figure 20).
- For MMICs operating at frequencies higher than 20 GHz, Coplanar waveguides (CPW) are typically used in place of microstrip lines.
- Transmission line models for each of these two categories are widely available and almost all of the modern microwave simulators include appropriate models, not only for 'straight runs' of lines, but also for common discontinuities such as bends, coupled lines, semi-circular lines, 'T' and cross junctions.
- Other shapes and structures of transmission lines may be used in MMIC as required. For such structures, detailed microwave modelling will be required for accurate prediction of circuit behaviour.

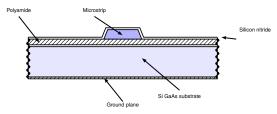
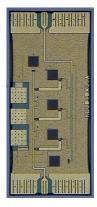


Figure 20 : MMIC microstrip line

MMIC application example

- A photomicrograph of a three-stage distributed amplifier MMIC is shown opposite.
- Each of the amplifying stages has two DHBT transistors configured as a cascode gain cell, that is, an input transistor in common emitter configuration, the output of which is connected to a transistor in common base configuration.
- The common-emitter devices are visible just at the top of the 'L'-shaped transmission lines and the common-base devices can be seen on the lower right of the same lines.
- A high impedance microstrip line, (Z_o = 70Ω), was used at the output of each gain cell to improve the bandwidth. The connections from the input transmission line to the common-emitter devices were designed to be as short as possible, since any inductance here reduces the gain and the bandwidth.
- The two devices in each gain cell are connected with an 'L'-shaped low impedance, low loss microstrip line.



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