Lecture 13 - Microwave Amplifier Design

Microwave Active Circuit Analysis and Design

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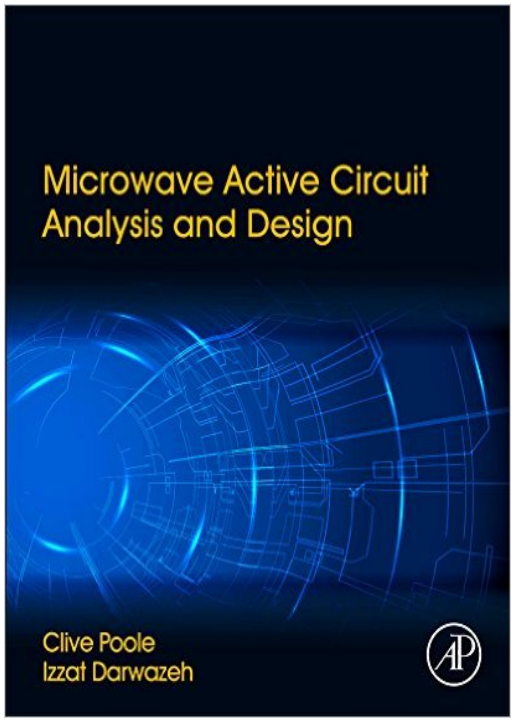

Intended Learning Outcomes

- Knowledge
  - Understand the operation of a single-stage microwave transistor amplifier.
  - Be familiar with the unilateral approximation, its application and limitations.
  - Understand the benefits of adding feedback in a transistor amplifier and be able to apply feedback design techniques to a single transistor amplifier.
- Skills
  - Be able to design a single-stage microwave transistor amplifier for maximum available gain.
  - Be able to apply constant gain circles to design a single-stage transistor amplifier to meet a particular gain specification.
  - Be able to design a feedback network to unilateralise a transistor.
  - be able to design a single-stage broadband transistor amplifier using resistive shunt/series feedback.
  - Be able to design a basic Distributed Amplifier (DA).

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Single-stage amplifier design

The simplest possible single-stage amplifier consists of a single transistor, a BJT in common emitter configuration, for instance, connected to a source and load both having the system characteristic impedance, Z_o as shown in figure 2.

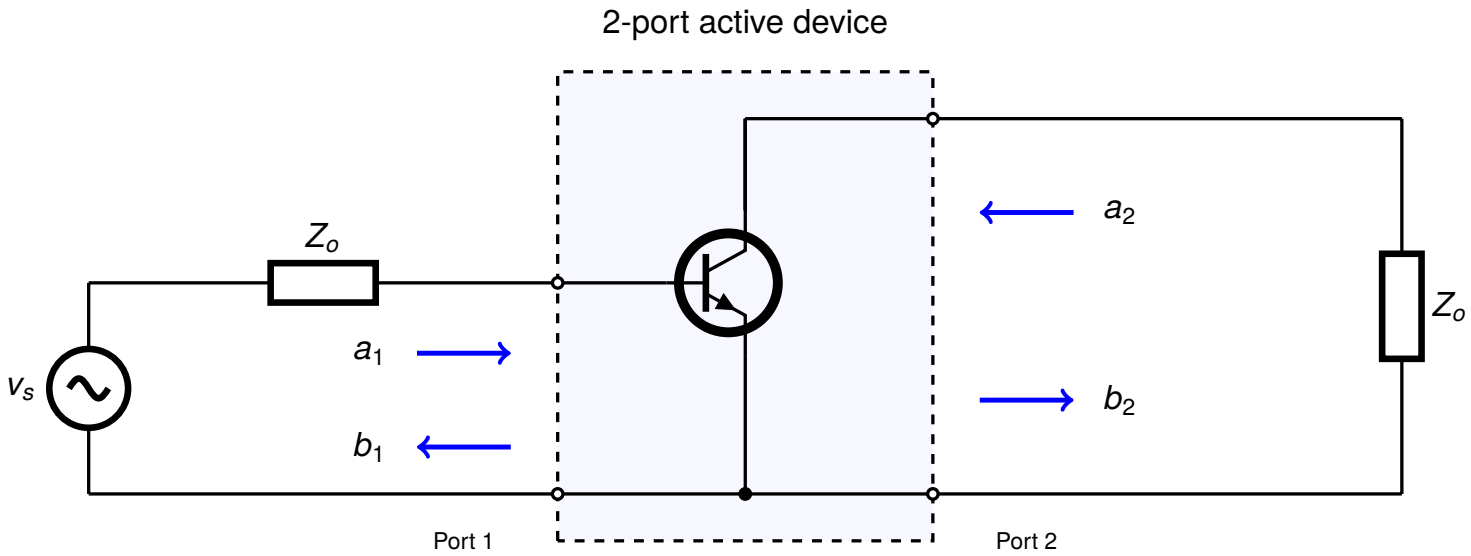


Figure 1 : The simplest possible single transistor amplifier

Single-stage amplifier design

We can write the relationship between the incident and reflected power waves at the input and output ports of the simple amplifier in figure 2 as follows :

$$b_1 = S_{11}a_1 + S_{12}a_2 \tag{1}$$

$$b_2 = S_{21}a_1 + S_{22}a_2 \tag{2}$$

One working definition of the power gain of this circuit is the ratio of the power entering at port 1 to the power emerging from port 2, with no power being incident at port 2. If we therefore set $a_2 = 0$ in (2) we can write the power gain of figure 2 as :

$$G = \frac{|b_2|^2}{|a_1|^2} = |S_{21}|^2 \tag{3}$$

This gain parameter is actually referred to as the *Transducer Power Gain*, or simply *Transducer Gain*, and is represented by G_T.

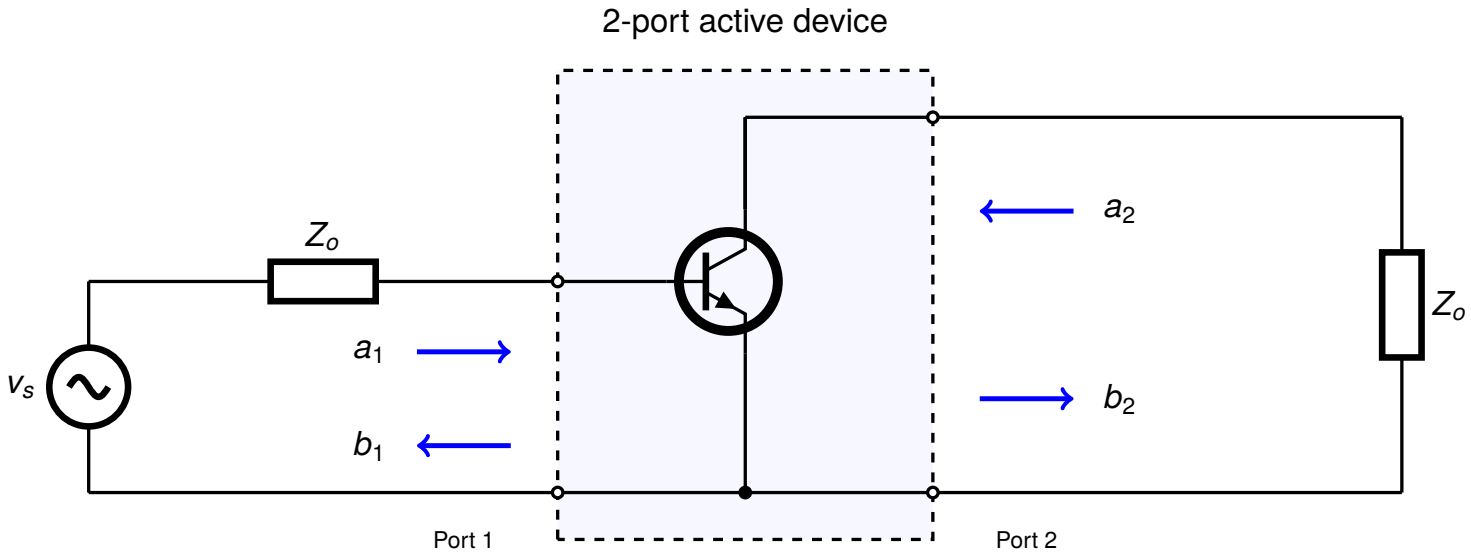


Figure 2 : The simplest possible single transistor amplifier

Single-stage amplifier design

We will now extend the simple case above to account for the more realistic situation of arbitrary source and load terminations, Z_S and Z_L (reflection coefficients Γ_S and Γ_L), as shown in figure 3.

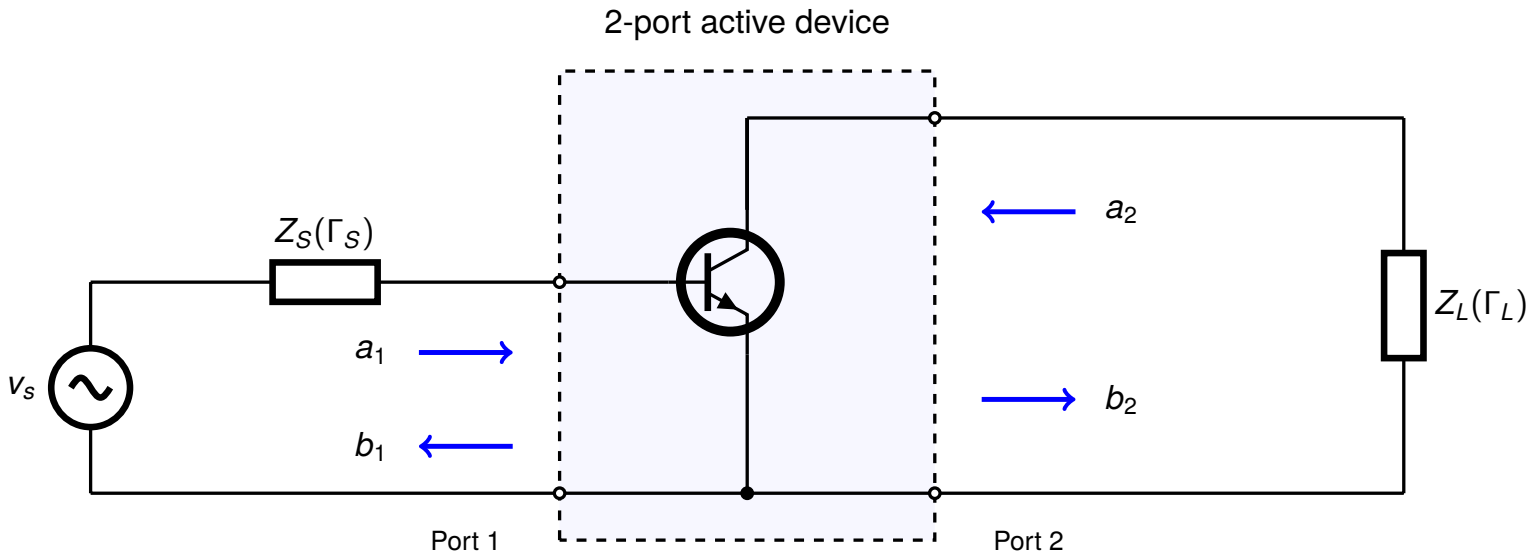


Figure 3 : Simple single transistor amplifier with arbitrary terminations

Single-stage amplifier design

In the case of the amplifier of figure 3, the simple transducer gain equation of (3) needs to be modified to account for the effects of impedance mismatch at both the input and output ports. We now need to write the equation for G_T for the circuit of figure 3 as follows :

$$G_T = M_S \times |S_{21}|^2 \times M_L \tag{4}$$

Where M_S and M_L are referred to as the *source mismatch factor* and *load mismatch factor*, respectively[2]. These 'mismatch factors' represent the amount of power actually delivered to the respective loads as a proportion of power available from the respective sources, in other words :

$$M_S = \frac{P_{in}}{P_{AVS}} \tag{5}$$

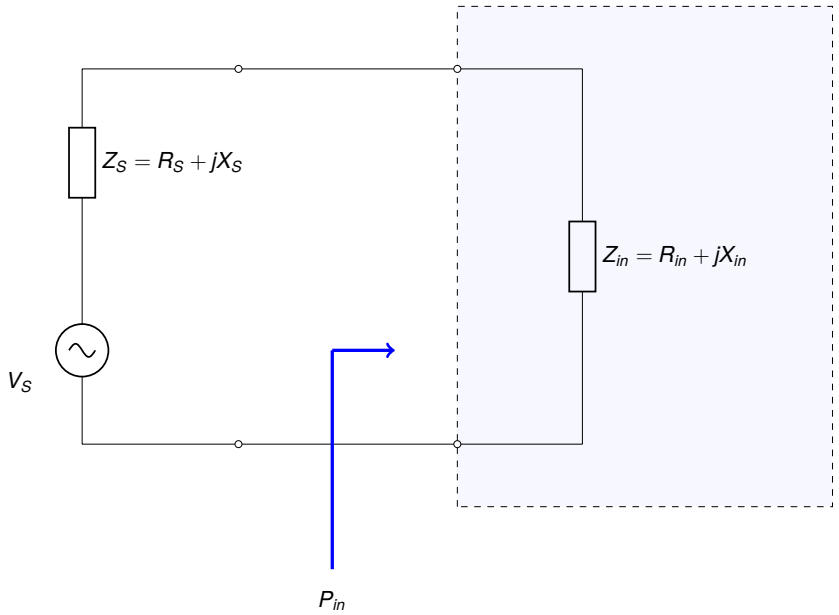
and

$$M_L = \frac{P_L}{P_{AVN}} \tag{6}$$

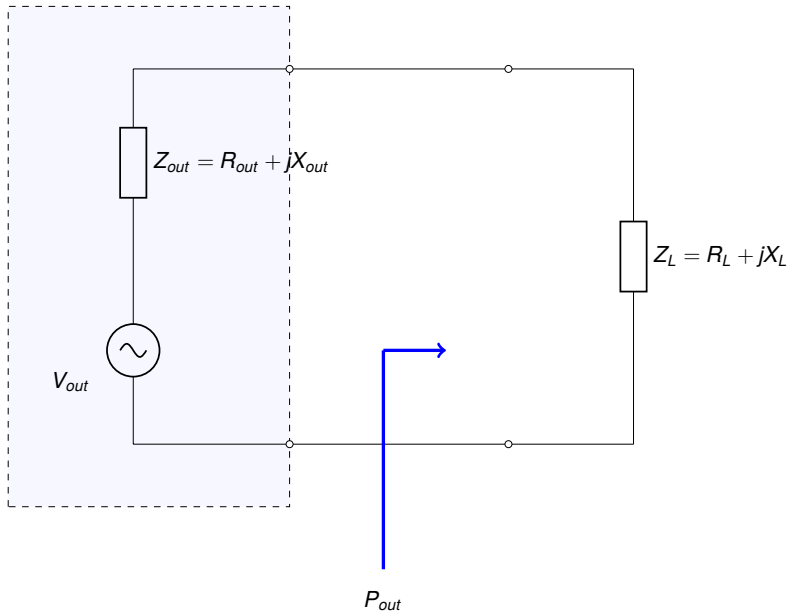
Where P_{AVS} is the power available from the source and P_{AVN} is the power available from the amplifier output port. Since P_{AVS} and P_{AVN} represent maximum power available from the respective sources (under conjugately matched conditions), we can therefore deduce that M_S and M_L can never be greater than unity.

Single-stage amplifier design

In order to express the mismatch factors in terms of termination impedances, we need to consider the power flow at the input and output of the amplifier separately, as shown in figure 4.



(a) Input port matching



(b) Output port matching

Figure 4 : Mismatch Factors

Single-stage amplifier design

We will first consider the situation at the input port, as shown in figure 4(a). The 'power available' from the source is defined as the power delivered into a conjugately matched load. If we consider the source in figure 4(a) as being conjugately matched to the input of the transistor, i.e. $Z_S = Z_{in}^*$, then the average power available from the source is :

$$P_{AVS} = \frac{1}{2}\frac{|V_S|^2}{R_S} \tag{7}$$

The power delivered to the input of the transistor in figure 4(a) is given by :

$$P_{in} = \frac{1}{2}\left|\frac{V_S}{Z_S + Z_{in}}\right|^2 R_{in} \tag{8}$$

By substituting (7) into (8), with some manipulation we get:

$$P_{in} = \frac{1}{8}\frac{|V_S|^2}{R_S}\left(\frac{4R_S R_{in}}{|Z_S + Z_{in}|^2}\right) = P_{AVS}\left(\frac{4R_S R_{in}}{|Z_S + Z_{in}|^2}\right) \tag{9}$$

Applying (9) to (5) we have :

$$M_S = \frac{4R_S R_{in}}{|Z_S + Z_{in}|^2} \tag{10}$$

Single-stage amplifier design

We shall now convert (10) to reflection coefficient form by applying (**??**). First, we write R_S in terms of Γ_S as follows :

$$R_S = \frac{1}{2}(Z_S + Z_S^*) = \frac{Z_o}{2}\left[\frac{1+\Gamma_S}{1-\Gamma_S} + \frac{1+\Gamma_S^*}{1-\Gamma_S^*}\right] = Z_o\frac{1-|\Gamma_S|^2}{|1-\Gamma_S|^2} \tag{11}$$

By similar reasoning we can express the real part of Z_{in} in terms of Γ_{in} :

$$R_{in} = Z_o\frac{1-|\Gamma_{in}|^2}{|1-\Gamma_{in}|^2} \tag{12}$$

By substituting (11) and (12) into (10), and replacing Z_S and Z_{in} in (10) by their reflection coefficient equivalents, we obtain the following expression for M_S in reflection coefficient terms :

$$M_S = \frac{(1-|\Gamma_{in}|^2)(1-|\Gamma_S|^2)}{|1-\Gamma_{in}\Gamma_S|^2} \tag{13}$$

A similar analysis to the above, applied to the output port of figure 4(b) results in a corresponding expression for the load mismatch factor, M_L :

$$M_L = \frac{(1-|\Gamma_{out}|^2)(1-|\Gamma_L|^2)}{|1-\Gamma_{out}\Gamma_L|^2} \tag{14}$$

Single-stage amplifier design

- From (14) we can deduce that for $M_L = 1$ the load must be conjugately matched to the output of the transistor, i.e. $\Gamma_L = \Gamma^*_{out}$. A quick look at (13) will similarly reveal that $M_S = 1$ when the source is conjugately matched to the input of the transistor, i.e. when $\Gamma_S = \Gamma^*_{in}$. This supports the intuitive understanding that the maximum available gain will be obtained from the transistor when we conjugately match the input and output ports.
- For any linear, non-unilateral, two-port, Γ_{in} will be dependent on the load termination and Γ_{out} will be dependent on the source termination, these quantities being related by (**??**) and (**??**). This means that for a non-unilateral device the mismatch factors M_S and M_L are interdependent.
- The ports cannot be conjugately matched independently as changing the value of Γ_L will alter the value of Γ_{in} and vice versa. In this case, we must employ a technique referred to as 'simultaneous conjugate matching' which was discussed in chapter **??**.

Single-stage amplifier design

The inter-relationship between the input and output ports of a non-unilateral two-port means that if we combine (13) and (14) together in a single gain expression, as in (4), we can eliminate one of either Γ_{in} or Γ_{out}. We therefore have a choice of two possible expressions for the transducer power gain that we obtain by substituting (13) and (14) into (4) and applying (**??**) and (**??**), as follows :

$$G_T = \frac{(1-|\Gamma_S|^2)}{|1-\Gamma_{in}\Gamma_S|^2}|S_{21}|^2\frac{(1-|\Gamma_L|^2)}{|1-S_{22}\Gamma_L|^2} \tag{15}$$

or :

$$G_T = \frac{(1-|\Gamma_S|^2)}{|1-S_{11}\Gamma_S|^2}|S_{21}|^2\frac{(1-|\Gamma_L|^2)}{|1-\Gamma_{out}\Gamma_L|^2} \tag{16}$$

The above equivalent expressions for transducer power gain, (15) and (16), were derived in chapter **??** and it was observed that they both consist of $|S_{21}|^2$ 'sandwiched' between the source mismatch factor and load mismatch factor, the latter two accounting for the degree of mismatch at the respective ports. The reader can easily confirm this by setting $\Gamma_S = 0$ and $\Gamma_L = 0$ in either (15) or (16), which will result in $G_T = |S_{21}|^2$ in both cases.

Generic Amplifier

- We have so far demonstrated that the gain performance of a transistor is a function of the source and load terminations, Γ_S and Γ_L, and that these terminations can be optimised to extract maximum gain from the transistor.
- In the real world we do not always have control over the sources and loads with which we are presented. We need a way to translate a given source and load to the terminating values we need at the transistor ports in order to achieve our specific performance requirements.
- In order to construct a practical amplifier, we need to add input and output matching networks in order to optimise gain, as well as bias networks to supply DC supply power to the transistor, as shown in figure 5.

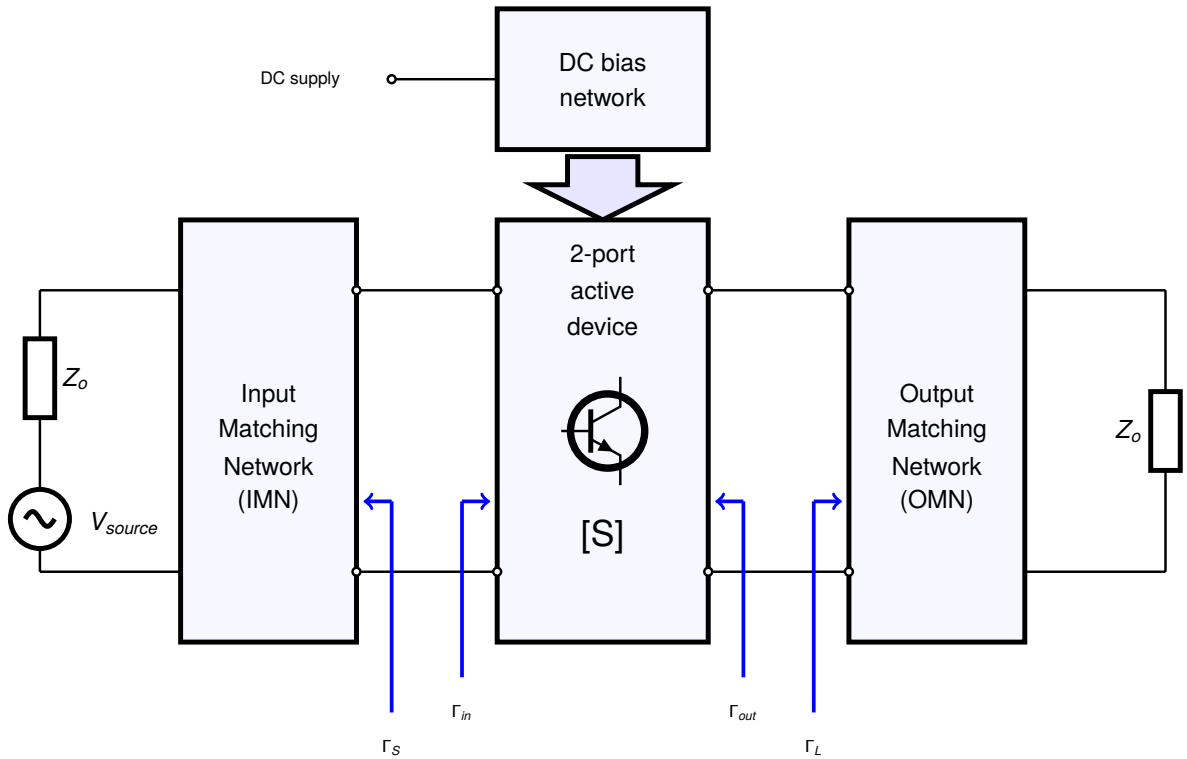


Figure 5 : Single active device with input and output matching network

The unilateral approximation

The parameter S_{12} represents internal feedback from the output to the input of a two-port device. In terms of the operation of practical amplifier circuits, it is desirable to have S_{12} as small as possible for two reasons:

1. The smaller the value of S_{12} the greater is the degree of isolation between the output and input A of a stage. This is an important consideration when stages are to be cascaded.
2. The smaller the value of S_{12} the greater is the degree of stability of a given stage.

However there is a third reason why a small value of S_{12} is desirable and it relates to the process of designing amplifier stages. If S_{12} is small enough we can make an approximation by setting $S_{12} = 0$ and the design process can be greatly simplified. This so called *Unilateral Approximation* also leads to greater conceptual simplicity when studying some of the factors which affect amplifier performance.

Of course, with practical transistors, $S_{12} \neq 0$ and any design procedure which assumes unilaterality will yield approximate results. The degree of error introduced by such an approximation can be quantified and a judgment can be made as to its acceptability in a given circumstance. Conditions close to unilaterality can be achieved by the application of feedback to a transistor, as will be discussed in Section **??**. Unilateral design techniques can be safely applied in such cases.

Unilateral Gain

We recall that the two alternative expressions for transducer power gain, given by equations (15) and (16), contain either the input reflection coefficient, Γ_{in} or the output reflection coefficient, Γ_{out}. In the case of a unilateral device, it is trivial to show, by means of setting $S_{12} = 0$ in (**??**) and (**??**), that $\Gamma_{in} = S_{11}$ and $\Gamma_{out} = S_{22}$. Both expressions for transducer power gain, (15) and (16), then reduce to the following single expression for Unilateral Transducer Power Gain, G_{TU} :

$$\boxed{G_{TU} = \frac{(1 - |\Gamma_S|^2)}{|1 - S_{11}\Gamma_S|^2} |S_{21}|^2 \frac{(1 - |\Gamma_L|^2)}{|1 - S_{22}\Gamma_L|^2}} \tag{17}$$

As we observed in the case of G_T, equation (17) is composed of the following three product terms:

$$G_{TU} = G_S \times G_o \times G_L \tag{18}$$

Where :

$$G_S = \frac{|1 - |\Gamma_S|^2|}{|1 - S_{11}\Gamma_S|^2} \tag{19}$$

$$G_o = |S_{21}|^2 \tag{20}$$

$$G_L = \frac{|1 - |\Gamma_L|^2|}{|1 - S_{22}\Gamma_L|^2} \tag{21}$$

Unilateral Gain

This time the mismatch factors, G_S and G_L, are independent of each other, meaning that the input and output ports of the device can be matched independently. G_S and G_L result from (13) and (14) when we set $\Gamma_{in} = S_{11}$ and $\Gamma_{out} = S_{22}$. G_o simply represents the transducer gain of the active device when terminated in the system characteristic impedance, Z_o.
It is a simple matter to show that, for a unilateral device, maximum gain is obtained when we set:

$$\Gamma_S = S_{11}^* \tag{22}$$

and

$$\Gamma_L = S_{22}^* \tag{23}$$

(17) then gives the value of the maximum unilateral gain as:

$$G_{TU_{max}} = \frac{1}{|1 - |S_{11}|^2|} |S_{21}|^2 \frac{1}{|1 - |S_{22}|^2|} \tag{24}$$

A further useful consequence of assuming unilaterality is that Rollett's stability factor tends to infinity and the stability criteria (**??**) simply reduce to:

$$\begin{aligned} |S_{11}| &< 1 \\ |S_{22}| &< 1 \end{aligned} \tag{25}$$

Circles of constant unilateral gain

Referring to the relationships (17) to (21), for a given device, $G_o = |S_{21}|^2$ is fixed so we only need consider the values of G_S and G_L, which depend on the values of Γ_S and Γ_L respectively.

Considering first (19), we note that G_S is maximum when the input port is conjugately matched, i.e. when $\Gamma_S = S_{11}^*$. In this case, we have $G_S = G_{S_{max}}$ where :

$$G_{S_{max}} = \frac{1}{1 - |S_{11}|^2} \tag{26}$$

We will define the normalised unilateral gain parameter, g_{Su} as :

$$g_{Su} = \frac{G_S}{G_{S_{max}}} = \frac{|1 - |\Gamma_S|^2|}{|1 - S_{11}\Gamma_S|^2}(1 - |S_{11}|^2) \tag{27}$$

Once again we note that the equation of a circle on the Γ_S plane is of the form :

$$|\Gamma_S - C_{gu}|^2 = |\gamma_{gu}|^2 \tag{28}$$

Where C_{gu} is the centre and γ_{gu} is the radius of the constant unilateral gain circle.

Circles of constant unilateral gain

We can thus rearrange equation (27) to be in the form of (28), as follows :

$$\left|\Gamma_S - \frac{g_{Su}S_{11}^*}{1-|S_{11}|^2(1-g_{Su})}\right|^2 = \left|\frac{\sqrt{1-g_{Su}}(1-|S_{11}|^2)}{1-|S_{11}|^2(1-g_{Su})}\right|^2 \tag{29}$$

By comparing (27) with (28), we determine the centers of the source plane constant unilateral gain circles as follows:

$$\boxed{C_{Su} = \frac{g_{Su}S_{11}^*}{1-|S_{11}|^2(1-g_{Su})}} \tag{30}$$

The radii of these circles are given by:

$$\boxed{\gamma_{Su} = \frac{\sqrt{1-g_{Su}}(1-|S_{11}|^2)}{1-|S_{11}|^2(1-g_{Su})}} \tag{31}$$

Circles of constant unilateral gain

We can carry out a similar analysis starting with (21) for G_L, which will lead us to the centres of the load plane constant unilateral gain circles as follows:

$$\boxed{C_{Lu} = \frac{g_{Lu} S_{22}^*}{1 - |S_{22}|^2(1 - g_{Lu})}} \tag{32}$$

The radii of these circles are given by:

$$\boxed{\gamma_{Lu} = \frac{\sqrt{1 - g_{Lu}}(1 - |S_{22}|^2)}{1 - |S_{22}|^2(1 - g_{Lu})}} \tag{33}$$

Where the normalised load plane unilateral gain parameter, g_{Lu}, is defined as :

$$g_{Lu} = \frac{G_L}{G_{L_{max}}} = \frac{|1 - |\Gamma_L|^2|}{|1 - S_{22}\Gamma_L|^2}(1 - |S_{22}|^2) \tag{34}$$

and

$$G_{L_{max}} = \frac{1}{1 - |S_{22}|^2} \tag{35}$$

Circles of constant unilateral gain

By inspection of equations (30), (31), (32) and (33) we can make the following observations about constant unilateral gain circles :

1. The angle of C_{Su} will always be equal to $\pm S_{22}$, which means that the centres of the constant unilateral gain circles on the source plane will always lie on the line drawn between S_{11}^* and the origin. Similarly, the centres of the constant unilateral gain circles on the load plane will always lie on the line drawn between S_{22}^* and the origin.
2. Maximum unilateral gain occurs when $g_{Su} = 1$ (i.e. when $G_S = G_{S_{max}}$). The source plane constant unilateral gain circle then reduces to a single point at S_{11}^* which corresponds to a conjugate match at the input port. The same applies to the output port.
3. When $g_{Su} = 1 - |S_{11}|^2$ or $G_S = 1$, we have $|C_{Su}| = |\gamma_{Su}|$. This indicates that the constant unilateral gain circle passes through the origin of the input reflection coefficient plane. This represents the boundary of the input network for providing gain, any values beyond this circle represent loss.

Error involved in the unilateral approximation

Making the assumption of unilaterality can result in a simplified design procedure. It is important, however, to be able to estimate the discrepancy between the results obtained by such a procedure and those obtained by using the unapproximated design equations introduced in the previous sections. A unilateral figure of merit has been proposed by, and named after, Mason[5] which is defined by:-

$$\boxed{U = \frac{|S_{11}S_{12}S_{21}S_{22}|}{(1-|S_{11}|^2)(1-|S_{22}|^2)}} \tag{36}$$

The quantity 'U' can be used to determine the maximum error associated with using G_{TU} instead of G_T in the design procedure, by using the following relationship:-

$$\frac{1}{(1+U)^2} \leq \frac{G_T}{G_{TU}} \leq \frac{1}{(1-U)^2} \tag{37}$$

The decision whether to apply the unilateral approximation is, of course, a matter of judgment. Typically, we can be comfortable using the approximation if the gain error, defined by the ratio $\frac{G_T}{G_{TU}}$ in (37), is within $\pm 10\%$, i.e. if $U < 0.05$. The interested reader is referred to an extensive treatment of the errors associated with assuming unilaterality published by Scanlan and Young [10].

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Single-stage feedback amplifier design

- The application of feedback to a two-port active device adds extra degrees of freedom in amplifier design, and allows us to achieve performance characteristics that would not be possible without feedback.
- We can apply the three port design techniques set out in chapter **??** to determine the effect of a given feedback termination on the S-parameters of the resulting 'reduced' two-port.
- We should recall that there are two types of feedback that can be applied to a single transistor, namely series feedback and shunt feedback, as shown in figure 6.

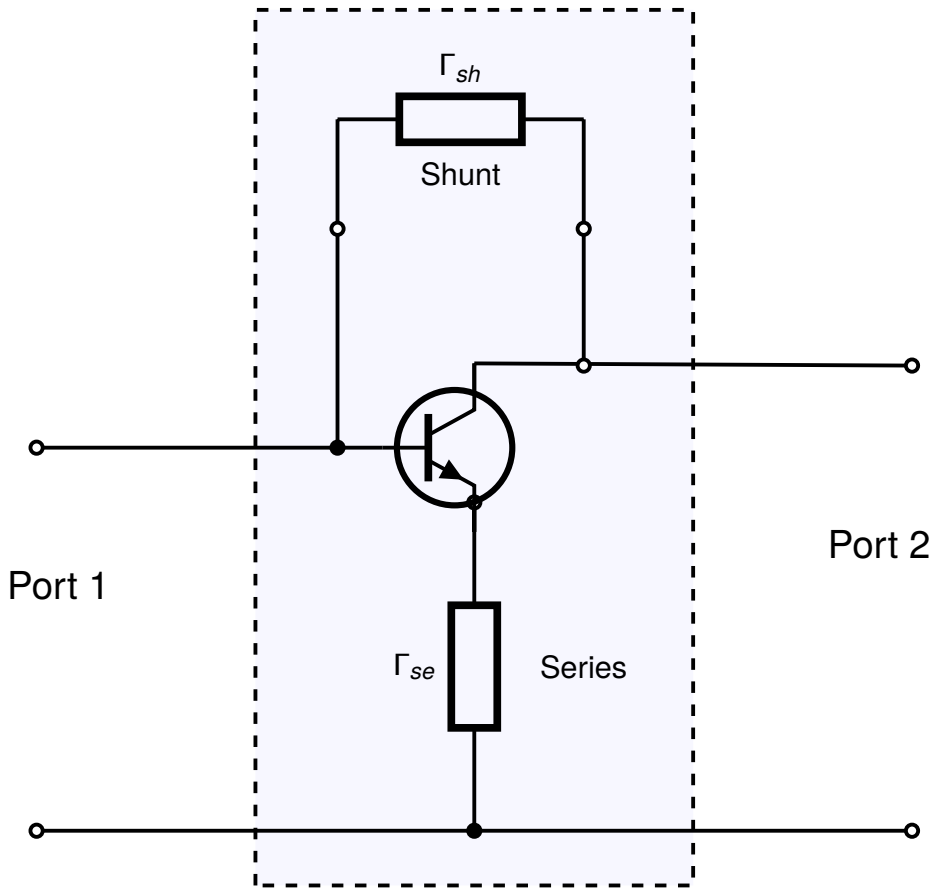

Figure 6 : Application of shunt and series feedback to a transistor

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Multi-stage amplifiers

- The gain of the single-stage amplifiers so far discussed is ultimately limited by the parameters of the transistor used.
- The conventional approach to increasing the gain above that of a single-stage is to cascade multiple stages.
- In order to achieve maximum power transfer between the stages, inter-stage matching networks are required, as shown in figure 7, that uses a BJT for illustration.

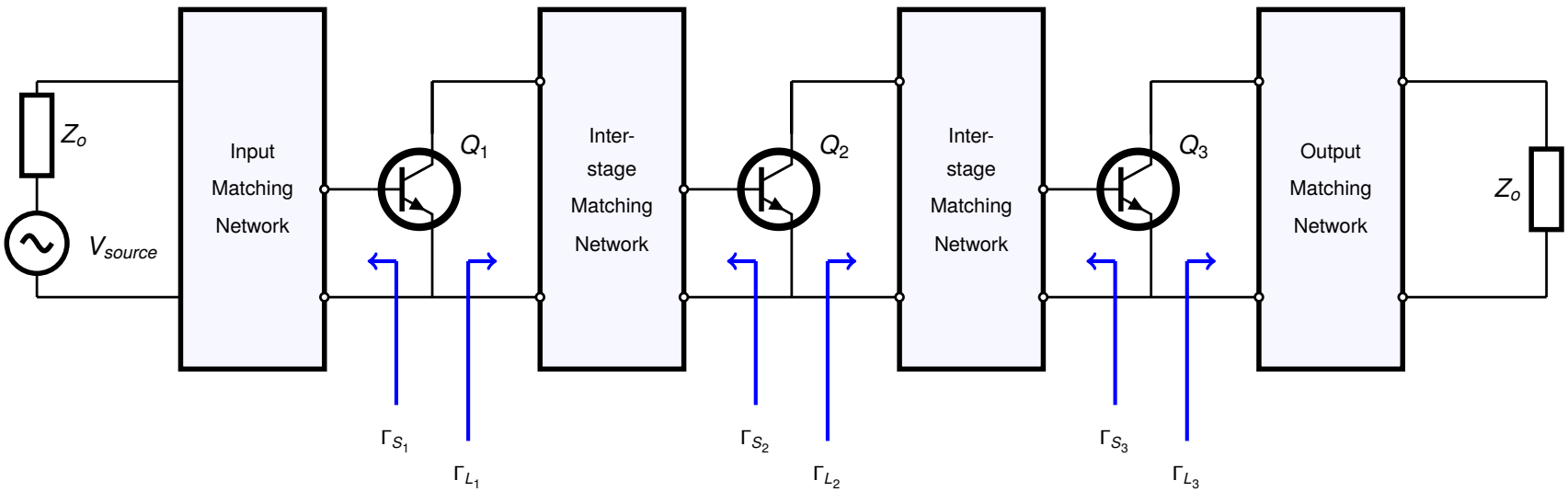


Figure 7 : Conceptual multi-stage amplifier

Multi-stage amplifiers

Ideally, with perfect lossless matching networks, the gain of a multi-stage amplifier is the product of the gains of each stage. The overall numeric gain of the amplifier in figure 7 is therefore :

$$G_{tot} = G_{Q_1} \cdot G_{Q_2} \cdot G_{Q_3} \tag{38}$$

If the gains are expressed in dB then (38) can be written as :

$$G_{tot(dB)} = G_{Q_1(dB)} + G_{Q_2(dB)} + G_{Q_3(dB)} \tag{39}$$

The individual stage gains in equations (38) and (39) will depend on the source and load terminations presented by the respective inter-stage matching networks (or input and output matching networks in the case of the first and last stages). Each transistor, Q_n, in figure 7 sees a source and load termination Γ_{S_n} and Γ_{L_n}, the values of which are determined by the respective matching network. Simplistically, we could maximise the gain of each stage by setting :

$$\Gamma_{S_n} = \Gamma_{ms_n} \tag{40}$$

and

$$\Gamma_{L_n} = \Gamma_{ml_n} \tag{41}$$

Where Γ_{ms_n} and Γ_{ml_n} are the optimum terminations for that particular transistor, defined by (**??**) and (**??**). This assumes, of course, that the device in question is unconditionally stable.

Multi-stage amplifiers

The design of the inter-stage matching networks is critically important to the performance of the overall amplifier and, consequently, a large body of work exists on this subject. In addition to fulfilling the gain specification, the design of the inter-stage matching circuitry must take into account several other requirements, such as:

- Impedance matching: As a general rule we seek to achieve maximum power transfer between each stage of a multi-stage amplifier. Exceptions to this rule are when we need to achieve minimum noise figure (as explained in chapter **??**) or when doing so would lead to instability of the overall amplifier.
- DC isolation: It is often the case that the output port of one stage is at a different DC potential to the input of the next, due to different bias requirements at base and collector (or gate and drain) terminals of a transistor. Each stage will therefore need to have DC isolation from the preceding and following stages. This is usually accomplished by means of a DC blocking capacitor. Depending on the capacitor value, its reactance may have to be incorporated in the AC analysis
- Frequency response: Attempting to satisfy the above two requirements will inevitably impact on a third important consideration, namely the frequency response of the overall amplifier. We often seek the maximum gain over the widest possible bandwidth and one approach is to eliminate any inter-stage coupling capacitors, which we would otherwise use for DC blocking. Such 'direct coupled' amplifiers are more challenging to design

Multi-stage amplifiers

A key figure of merit which is particularly important for multi-stage amplifiers is the *Gain-Bandwidth Product* or 'GBP', which is defined as the product of the amplifier's 3dB bandwidth and the nominal gain (i.e. the gain at the centre of the passband).

Since gain is a dimensionless ratio (not dB), the gain-bandwidth product is expressed in units of Hz. For the purposes of this analysis, we shall assume that the amplifier has a first-order frequency response, described by:

$$A(\omega) = \frac{A_o}{\sqrt{1 + \left(\frac{\omega}{\omega_c}\right)^2}} \tag{42}$$

Where A_o is the nominal or 'pass band' gain of the amplifier and ω_c is the corner frequency of the first order response, i.e. the 3dB frequency.

We can show that the GBP is approximately constant, in other words gain and bandwidth can be 'traded-off' against each other, as follows, starting with the definition of GBP at a frequency, ω :

$$GBP = A(\omega) \cdot \omega \tag{43}$$

$$= \frac{A_o}{\sqrt{1 + \left(\frac{\omega}{\omega_c}\right)^2}} \cdot \omega \approx \frac{A_o}{\sqrt{\left(\frac{\omega}{\omega_c}\right)^2}} \cdot \omega \tag{44}$$

$$= A_o \cdot \omega_c \tag{45}$$

Since both A_o and ω_c are constants, it follows that $A_o \cdot \omega_c$ must be a constant.

For transistors, the current gain-bandwidth product is the same as the transition frequency, f_T, that was defined for BJTs and FETs in (**??**) and (**??**), respectively.

Multi-stage amplifiers

When designing multi-stage amplifiers, we encounter the problem of *bandwidth shrinkage*. This is due to the fact that the gain versus frequency transfer functions are multiplied, increasing the overall gain but also increasing the steepness of the gain roll-off. We therefore need to be aware that, as we increase the gain by adding more stages, we will inevitably be sacrificing bandwidth.

Consider a multi-stage amplifier, such as that shown in figure 7, generalised to n identical stages, each having a voltage gain A and a 3dB bandwidth B.
Let us again assume a 'first order' frequency dependence for the individual stages, so that the frequency dependence of amplifier gain magnitude for each stage is represented by:

$$A(f) = \frac{A_o}{\sqrt{1 + \left(\frac{f}{B}\right)^2}} \tag{46}$$

For the overall amplifier consisting of n such stages in cascade we have, from an extension of (38) to n stages :

$$A_t(f) = \left[\frac{A_o}{\sqrt{1 + \left(\frac{f}{B}\right)^2}}\right]^n \tag{47}$$

Multi-stage amplifiers

With an amplifier having a first order response, the overall 3dB bandwidth of the amplifier is the frequency at which the voltage gain falls to $1/\sqrt{2}$ of its nominal value, A_t, i.e. where $A_t(f) = A_t/\sqrt{2}$. At this frequency, which we will call B_t, and based on (47) we can write:

$$\frac{A_t}{\sqrt{2}} = \left[\frac{A_o}{\sqrt{1+\left(\frac{B_t}{B}\right)^2}}\right]^n \tag{48}$$

Given that $A_t = A_o^n$, we can derive the bandwidth of the overall amplifier in terms of the individual stage bandwidths from (48) as:

$$B_t = B\sqrt{2^{1/n}-1} \tag{49}$$

A cascade of n identical amplifier stages will therefore have a bandwidth less than that of an individual stage by a factor of $\sqrt{2^{1/n}-1}$. The gain-bandwidth product for each individual stage can thus be written as :

$$GBP_S = A_o \times B = \left(\frac{B_t}{\sqrt{2^{1/n}-1}}\right) \cdot (A_t)^{1/n} \tag{50}$$

Multi-stage amplifiers

An interesting question arising from equation (50) is, what is the optimum number of stages which will be required to achieve the maximum overall GBP specification for a cascade of identical amplifier stages? Jindal [3] answered this question by differentiating (50) with respect to n and obtaining the optimum number of stages, n_{opt}, as a function of the overall gain, A_t, as follows :

$$n_{opt} = \frac{\ln(2)}{-\ln\left[-\frac{\ln(2)}{2\ln(A_t)}\right]} \tag{51}$$

If $A_t >> \sqrt{2}$ we can approximate 51 to :

$$n_{opt} = 2\ln(A_t) \tag{52}$$

Jindal [3] gives the example of a multi-stage amplifier having a gain $A_t = 100$, for which (52) gives $n_{opt} = 9.2$. If we required the overall amplifier to have a bandwidth of 880 MHz, we find that the optimum value for the GBP for each individual stage, from (50) is 5.2 GHz.

Fundamental limits on inter-stage matching networks

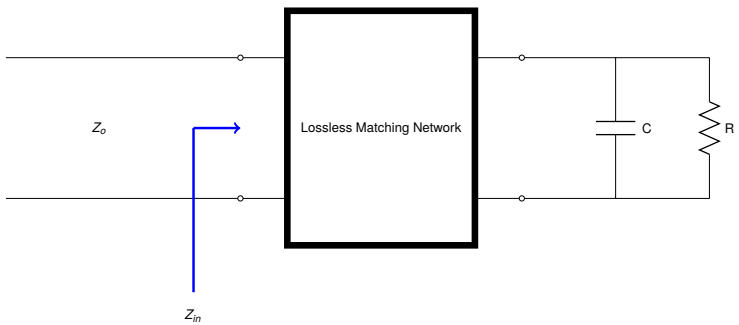
When designing a lossless matching network to match an arbitrary complex load, the following questions arise :

- Is it possible to achieve a perfect match (i.e zero reflections) over a specified bandwidth?
- If not, what are the trade-offs between quality of match (i.e. reflection coefficient) and bandwidth?
- How complex must the matching network be for a given specification?

The **Bode-Fano Criterion** gives a theoretical limit on the minimum reflection magnitude (or optimum result) for an arbitrary matching network. The criterion provides the theoretical upper limit of performance that can be obtained. This gives us a benchmark and allows us to trade off between reflection coefficient, bandwidth, and network complexity.

For example, the Bode-Fano criterion for a parallel RC load is :

$$\int_0^x \frac{1}{|\Gamma(\omega)|}\, d\omega \leq \frac{\pi}{RC}$$



Bode-Fano Limits for RC loads

Shown here are the Bode-Fano limits for RC loads matched with passive and lossless networks (ω_o is the center frequency of the matching bandwidth) :

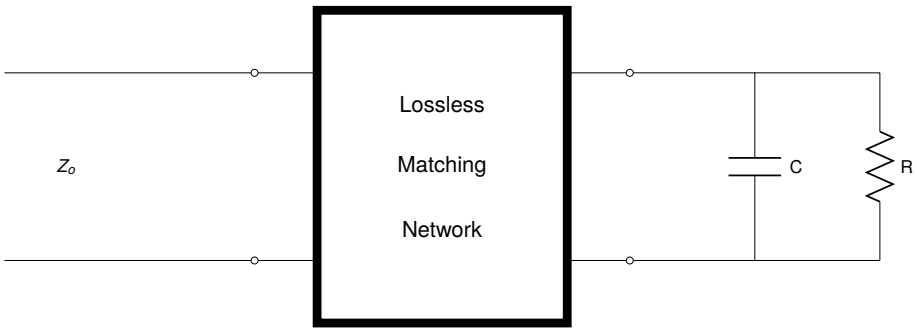


Figure 8 : Bode Fano Criterion : parallel RC

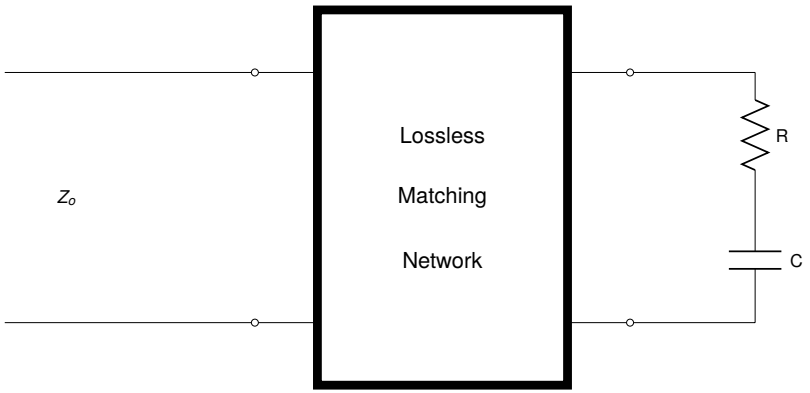


Figure 9 : Bode Fano Criterion : Series RC

$$\int_0^\infty \frac{1}{|\Gamma(\omega)|}\, d\omega \leq \frac{\pi}{RC}$$

$$\int_0^\infty \frac{1}{|\Gamma(\omega)|}\, d\omega \leq \pi\omega_o^2 RC$$

Bode-Fano Limits for RL loads

Shown here are the Bode-Fano limits for RL loads matched with passive and lossless networks (ω_o is the center frequency of the matching bandwidth) :

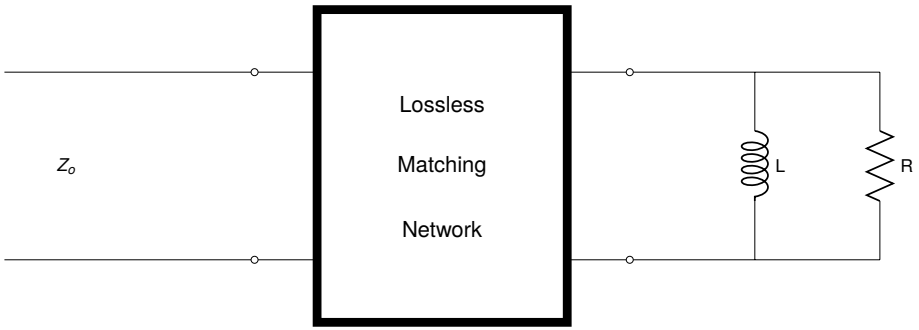


Figure 10 : Bode Fano Criterion : parallel LC

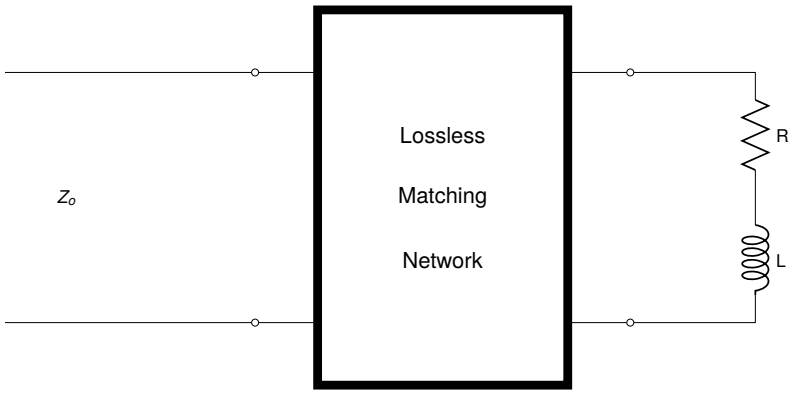


Figure 11 : Bode Fano Criterion : Series RL

$$\int_0^\infty \frac{1}{|\Gamma(\omega)|}\, d\omega \leq \frac{\pi \omega_o^2 L}{R}$$

$$\int_0^\infty \frac{1}{|\Gamma(\omega)|}\, d\omega \leq \frac{\pi R}{L}$$

Bode-Fano Criterion

The Bode-Fano limits can be written in terms of reactance/susceptance for a generalised load impedance/admittance respectively as follows:

$$\frac{\Delta\omega}{\omega_o}\frac{1}{\Gamma_{avg}} \leq \frac{\pi G}{B} \tag{53}$$

$$\frac{\Delta\omega}{\omega_o}\frac{1}{\Gamma_{avg}} \leq \frac{\pi R}{X} \tag{54}$$

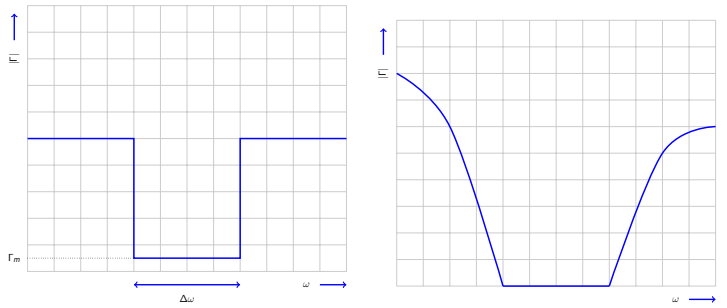
where G is the load conductance, B is the load susceptance, R is the load resistance and X is the load reactance.

The load that was initially considered by Bode was the simple parallel RC circuit shown in figure **??**. In this case, the match performance limit can be described in terms of load-Q, as follows:

$$\frac{\Delta\omega}{\omega_o}\frac{1}{\Gamma_{avg}} \leq \frac{\pi}{Q} \tag{55}$$

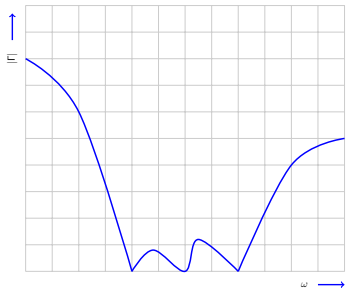
Bode-Fano Criterion

- Equation (55) suggests that the more reactive energy that is stored in a load, the narrower the bandwidth of a match. The higher the Q is, the narrower the bandwidth of the match for the same average in-band reflection coefficient. Accordingly, it will be much harder to design the matching network to achieve a specified matching bandwidth. Only when the load is purely resistive can a match over all frequencies be found.
- The ideal situation is to maintain $1/\Gamma$ constant over the frequency range of interest, $\Delta\omega$ and have it equal to one outside this range, as shown in figure 12(a). A matching profile like that of figure 12(a) is unrealisable as it would require an infinite number of elements in the matching network[8].
- Even a more realistic response like that shown in figure 12(b) is unrealisable as it is not possible in practice to achieve a perfectly flat passband response.
- Any realisable matching network will have a response resembling the one shown in figure 12(c), where neither the passband or stopband response are 'ideal'.



(a) Idealised matching network response

(b) Non-realisable matching network response



(c) Realisable matching network response

Figure 12 : Bode-Fano matching illustration

Implications of the Bode-Fano Criterion

The implications of the Bode-Fano criterion as follows :

- For a given load, (e.g. a fixed RC product) broader bandwidth ($\Delta\omega$) can be achieved only at the expense of higher reflection coefficient in the passband.
- The reflection coefficient in the passband cannot be zero unless $\Delta\omega = 0$. Thus a perfect match can be achieved only at a finite number of frequencies.
- As R and/or C increases, the quality of the match ($\Delta\omega = 0$ and/or $1/\Gamma_m$) must decrease. Thus higher-Q circuits are intrinsically harder to match than are lower-Q circuits.

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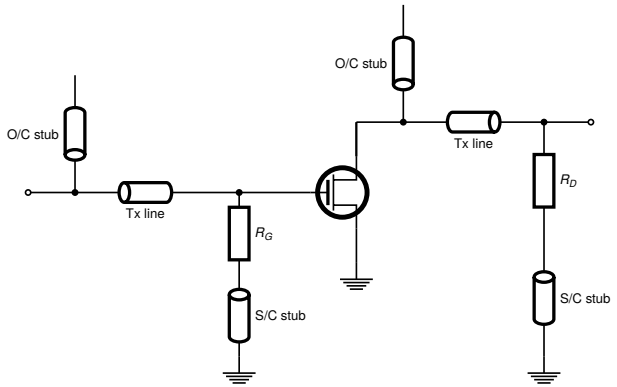
Broadband amplifiers

In the previous section, we looked at the essential trade-off between gain and bandwidth in multi-stage amplifiers, i.e. as we cascade more and more stages to achieve higher gain, the overall bandwidth of the amplifier inevitably 'shrinks'. In the ongoing quest for wider and wider bandwidths, a number of strategies have been developed to overcome the limitations of the conventional multi-stage amplifier approach exemplified by figure 7.
Three broadband amplifier topologies are particularly well suited to MMIC implementation, so we will focus on these as follows[11]:

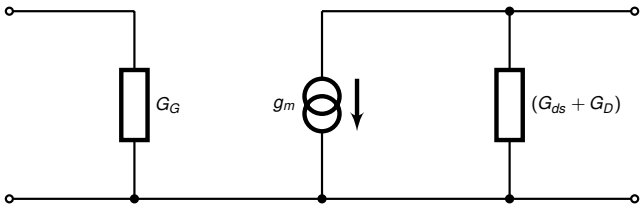
1. Lossy Matched Amplifier(LMA): Where lossy elements (i.e. resistors) are used to achieve good input, output and inter-stage matching across a wide range of frequencies
2. Feedback amplifiers: Where negative feedback is applied to extend the bandwidth. Both shunt and series feedback configurations have been used in this context but shunt feedback usually yields the best results.
3. Distributed amplifiers: Which employ the concept of 'additive amplification' and offer ultra-broadband operation that can extend from DC up to the cut-off frequency of the active devices.

Lossy matched amplifiers

- A lossy match amplifier (LMA) uses resistors within its matching networks to enable flat gain to be achieved over a broad bandwidth.
- The most common topology employs resistors in series with high impedance stubs on both the input and output, as shown in figure 13(a)[9], where a FET has been used for example and the matching networks consist of a mixture of resistors and transmission line stubs.
- At low frequencies, the stubs have little reactance, so the resistors form the major part of the load on the transistor, lowering its gain.
- At higher frequencies, the reactance of the stubs increases (tending to infinity when the stubs are a quarter-wavelength long), and the resistors have less effect on the transistor gain. Hence, the matching networks can introduce a positive gain slope to compensate the transistor's gain roll-off, without resorting to mismatching.
- Lossy match amplifiers have moderate gain and acceptable gain flatness. The use of resistors also enhance the stability of the amplifier at low frequencies. The downside of the lossy matching approach, compared to reactively matched amplifiers, are lower gain, lower output power and higher noise figure, as the resistors add thermal noise.



(a) Basic lossy matching topology



(b) Low frequency model

Figure 13 : Lossy matching of a FET amplifier

Lossy matched amplifiers

Niclas[6, 7] uses the the low frequency model of a lossy match FET amplifier, shown in figure 13(b), to illustrate lossy matching. From figure 13(b) it can be seen that :

$$S_{11} = \frac{1 - G_G Z_o}{1 + G_G Z_o} \tag{56}$$

$$S_{22} = \frac{1 - (G_{ds} + G_D) Z_o}{1 + (G_{ds} + G_D) Z_o} \tag{57}$$

and

$$Gain \approx \left[\frac{g_m Z_o}{2} (1 + S_{11})(1 + S_{22}) \right] \tag{58}$$

where G_{ds} is the drain-source conductance $(1/R_{ds})$ and G_D is the lossy match drain loading conductance.

From equation (58), it can be seen that if $G_G = (G_{ds} + G_D) = 1/Z_o$ (i.e. the gate loading resistor is 50Ω) and the drain loading resistor in parallel with R_{ds} gives 50Ω, then $S_{11} = 0$, $S_{22} = 0$ and the gain (in dB) is equal to $20log((g_m Z_o)/2)$, which gives typically 8 dB for an 800 μm MESFET. This low frequency model clearly shows how the gate-width of the FET determines the low frequency gain of the lossy match amplifier in the ideally matched case.

Broadband feedback amplifiers

An example of a multi-stage MESFET amplifier employing shunt voltage feedback to extend the bandwidth of the first stage is shown in figure 14.

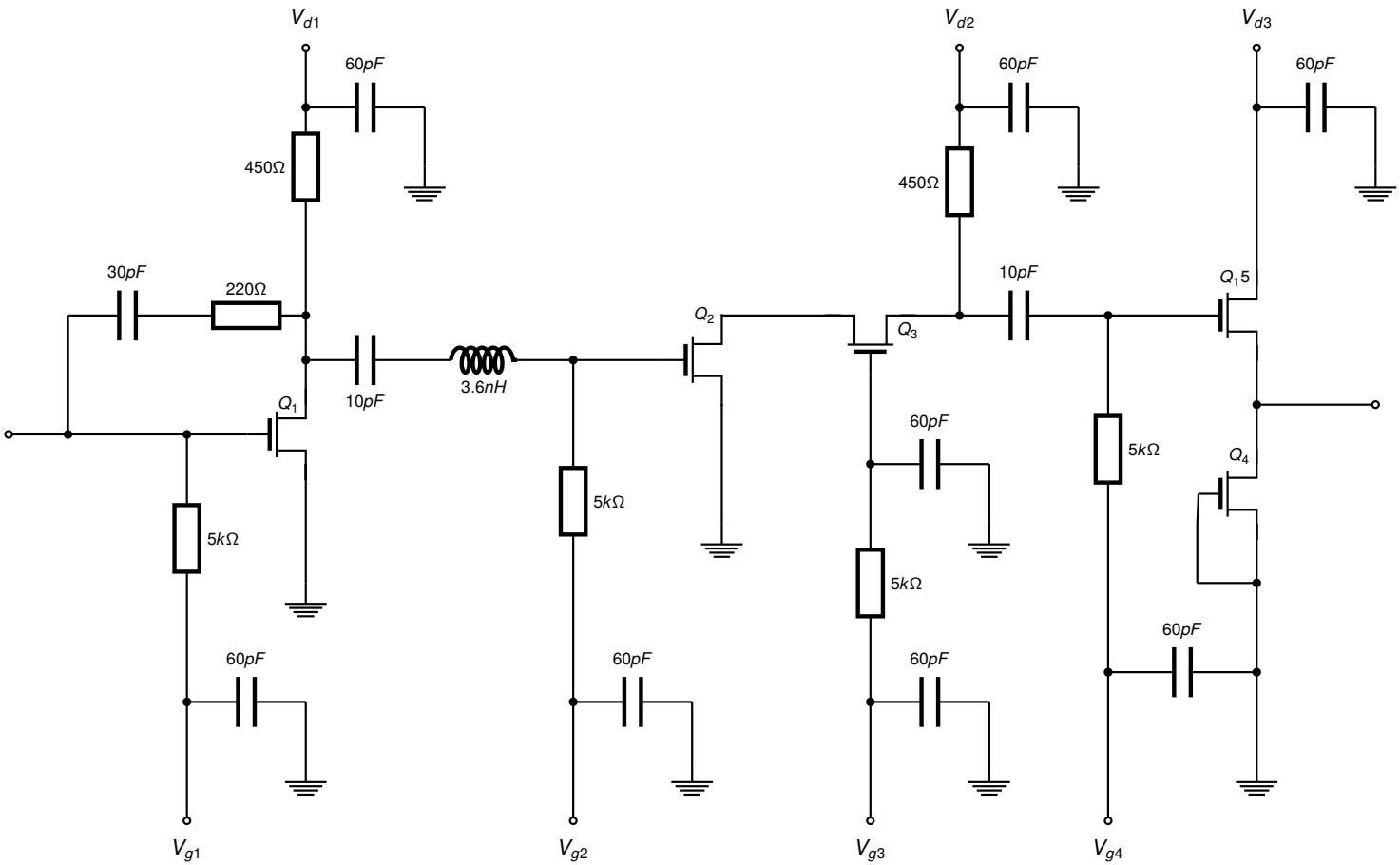


Figure 14 : Common Source (2.4 Gbit/s) MMIC feedback amplifier

Broadband feedback amplifiers

The circuit shown in figure 15 is an enhancement of the circuit of figure 14 using shunt feedback networks around both the first and second stages.

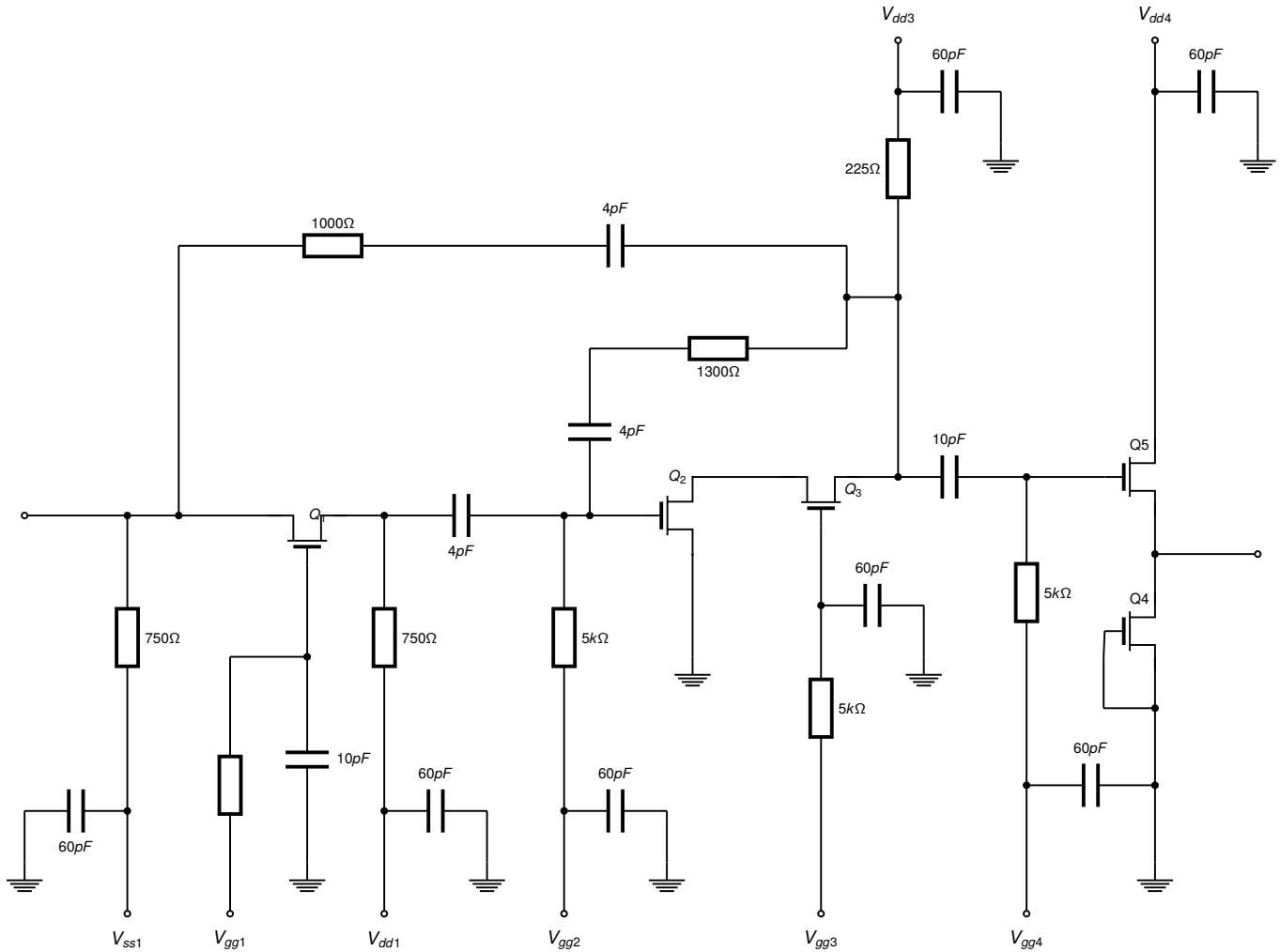


Figure 15 : Common Gate (5 Gbit/s) MMIC feedback amplifier

Distributed Amplifiers

- The basic conceptual architecture of a distributed amplifier consists of a pair of transmission lines, shown as the upper and lower line in figure 16.
- An input signal injected into the lower transmission line will propagate down the line and will arrive at the terminating resistor, R_1, which is a matching resistor having the same value as the line characteristic impedance, Z_o.
- As the signal propagates along the lower transmission line, the inputs of the individual gain stages are driven with a particular phase relationship to each other, determined by their position along the line.
- The input signal is amplified by each gain stage, and the stage outputs are combined coherently (i.e. with their phase relationships preserved) in the upper transmission line.
- The propagation characteristics of the upper and lower transmission lines in figure 16 must be designed to be equal so as to ensure that output signals from each individual gain stage sum in phase.

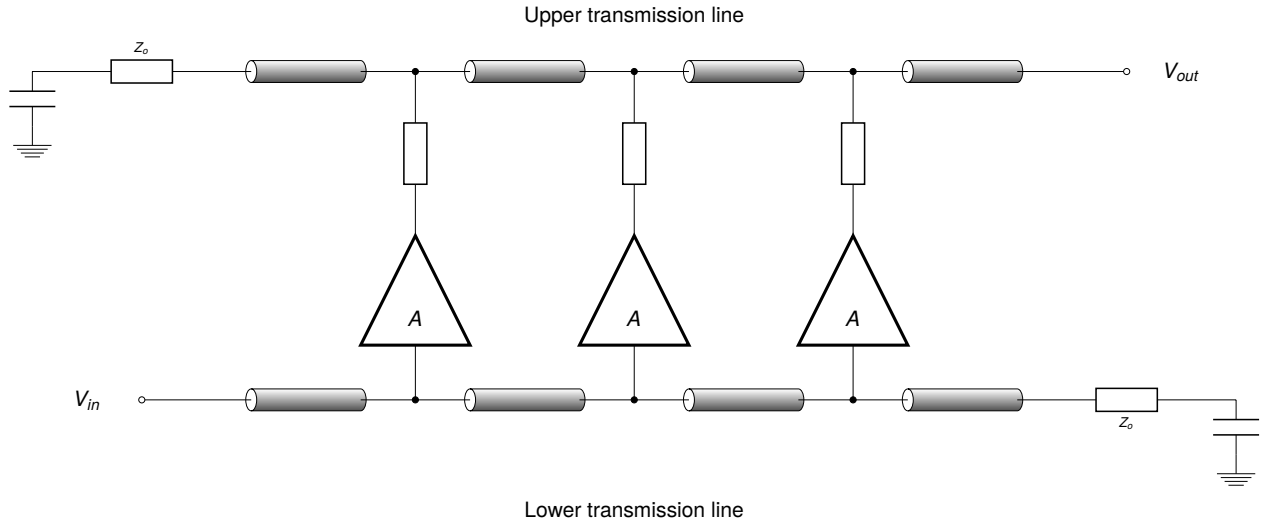


Figure 16 : Conceptual distributed amplifier architecture

Distributed Amplifiers

- The gain stages in figure 16 can be implemented as single transistor amplifiers, as illustrated in figure 17, which shows the basic AC circuit of a distributed amplifier with N identical transistor amplifier stages.
- The active devices are shown in figure 17 are MESFETs or HEMTs, but the following description applies equally to bipolar transistors(BJT or HBT).

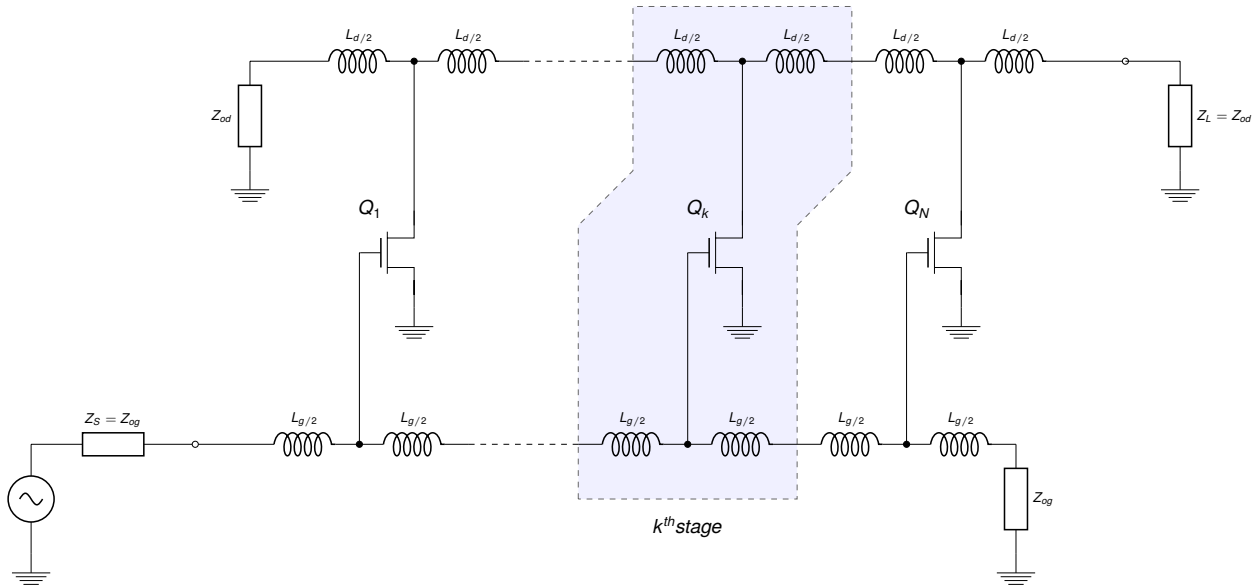


Figure 17 : Basic AC circuit schematic of an N-stage MESFET distributed amplifier

Distributed Amplifiers

- Figure 18(b) and 18(c) depict the simplified small-signal equivalent circuit models for the input and output portions of a MESFET Distributed Amplifier respectively.
- The current source in parallel with C_{ds} in figure 18(c) represents the intrinsic current that is generated by a MESFET through its gain mechanism. g_m is the complex transconductance which, when multiplied by the input voltage v_{gs} developed across C_{gs}, gives the value of the drain current produced internally by the MESFET.
- L_g and L_d are the total inductances present between the input base and output collector terminals of adjacent transistors, respectively.

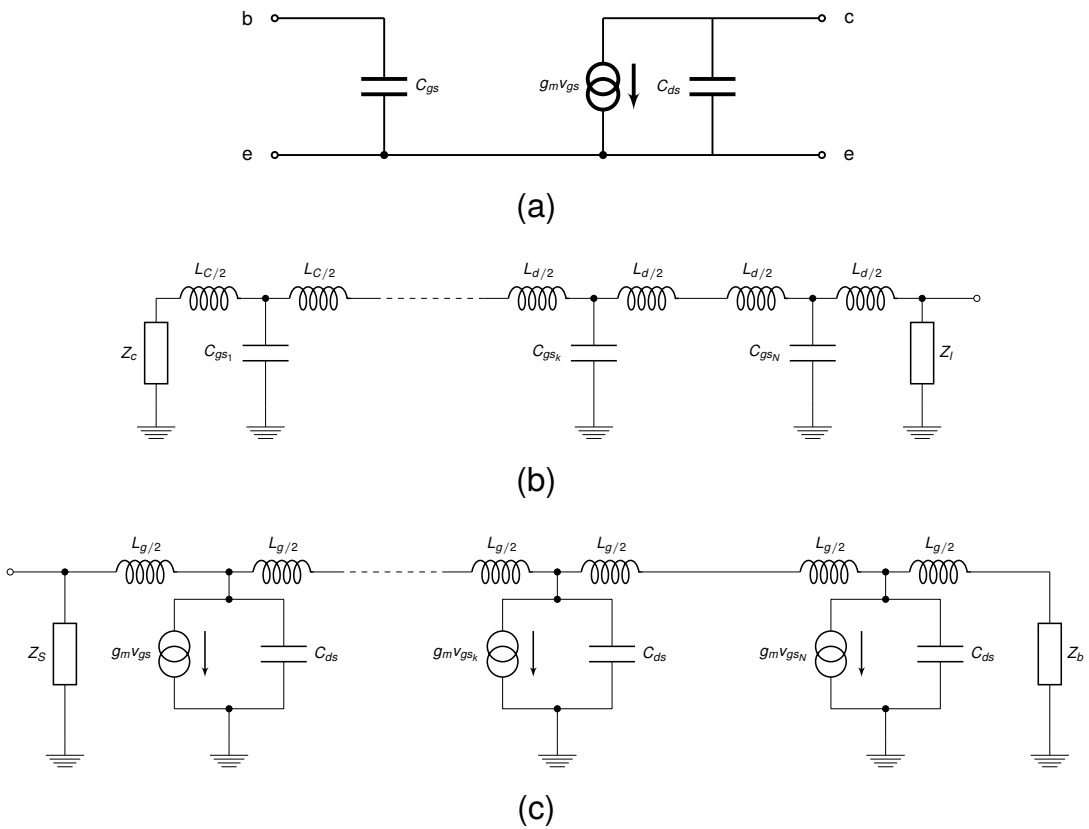


Figure 18 : Simplified small-signal equivalent circuit models of MESFET based Distributed Amplifier artificial transmission lines: (a) Individual MESFET equivalent circuit (b) Gate-line equivalent circuit (c) Drain-line equivalent circuit

Distributed Amplifiers

- An ideal uniform lossless transmission line can be represented by an equivalent electrical model consisting of a distributed total series inductance ΔL and a distributed shunt capacitance ΔC[4], as depicted in Figure 19.
- The quantities ΔL and ΔC are termed 'distributed' because they are defined per unit length of transmission line. If we compare figure 18 with figure 19 we notice that the input and output portions of a distributed amplifier each resemble the equivalent circuit model of a lossless transmission line. Consequently, a direct analogy can be established between the two circuit portions of a Distributed Amplifier and a transmission line where the transistor parasitic capacitances, C_π and C_{ce}, are incorporated into what is, in effect, an *Artificial Transmission Line* (ATL).
- A distributed amplifier can essentially be viewed as a pair of transmission lines, coupled via the active devices and thus possess amplifying properties.

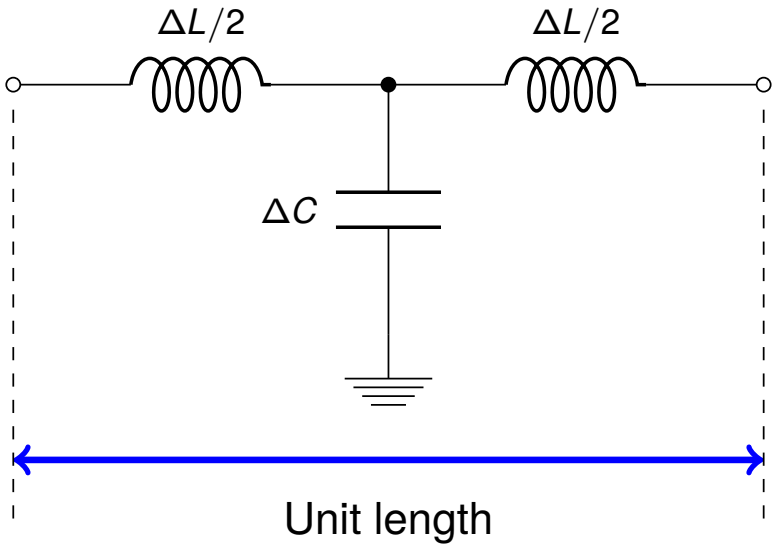


Figure 19 : Unit length element of an ideal uniform lossless real transmission line

Distributed Amplifiers

Ideally, the gain of a Distributed Amplifier can be made larger by increasing the number of amplifier sections, while bandwidth is preserved since it is fixed by the cut-off characteristics of the ATLs. By virtue of the independence of the amplifier properties that set bandwidth and gain, the GBP of a distributed amplifier may even exceed f_T of the active devices themselves.

Having ignored R_i and R_{ds} in the MESFET equivalent circuits, the gain of the amplifier is given by[1]:

$$G = \frac{1}{4} N^2 g_m^2 Z_{og} Z_{od} \tag{59}$$

Where N is the total number of stages and Z_{og} and Z_{od} are the characteristic impedances of the gate and drain ATLs, respectively, and are therefore the values of the terminating impedances employed in figure 17. These characteristic impedances are given by:

$$Z_{og} = \sqrt{\frac{L_g}{C_{gs}}} \tag{60}$$

$$Z_{od} = \sqrt{\frac{L_d}{C_{ds}}} \tag{61}$$

Distributed Amplifiers

Equation (59) would seem to suggest that it is possible to increase the amplifier gain by simply increasing the number of stages. The losses introduced by R_i and R_{ds}, however, which we have ignored in this analysis so far, result in an optimum number of stages to maximise the gain for a given active device[1]. In theory, the gain of a DA should remain flat up to the f_T of the active devices, provided that the cut-off frequency of the ATLs is made much higher than the device f_T. The cut-off frequencies of the gate and drain ATLs are given by:

$$f_{cg} = \left(\frac{1}{\pi \sqrt{L_g C_{gs}}} \right) \tag{62}$$

$$f_{cd} = \left(\frac{1}{\pi \sqrt{L_d C_{ds}}} \right) \tag{63}$$

A consequence of the above equations (60), (61), (62) and (63), is that, once the characteristic impedance of the ATL has been chosen then the cut-off frequencies cannot be chosen independently. Up till now we have considered the use of matching networks to interconnect circuits having different characteristic impedances. In the case of distributed amplifiers, which are by their nature extremely broadband, the characteristic impedance of the ATLs that make up the distributed amplifier are constrained by the need to match directly to preceding and subsequent circuits.

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